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Special Report:

EDN's μP/μC directory exposes unsupported benchmarks

pg 90

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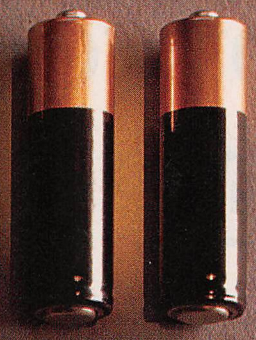

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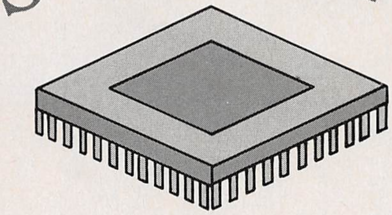


Microprocessor DIRECTORY

Benchmarks don't have to be confusing and deceptive. Application code that bears a resemblance to your software, consistently applied across a range of similarly configured microprocessor-based systems, can be useful in selecting your hardware.

Michael C Markowitz, *Associate Editor*

> Most microprocessor vendors use benchmarks as a drunken man uses lampposts—for support rather than illumination.
>
> *—Adapted from Andrew Lang, Scottish author*

> There are three kinds of lies: lies, damned lies, and benchmarks.
>
> *—Adapted from Benjamin Disraeli, British statesman*

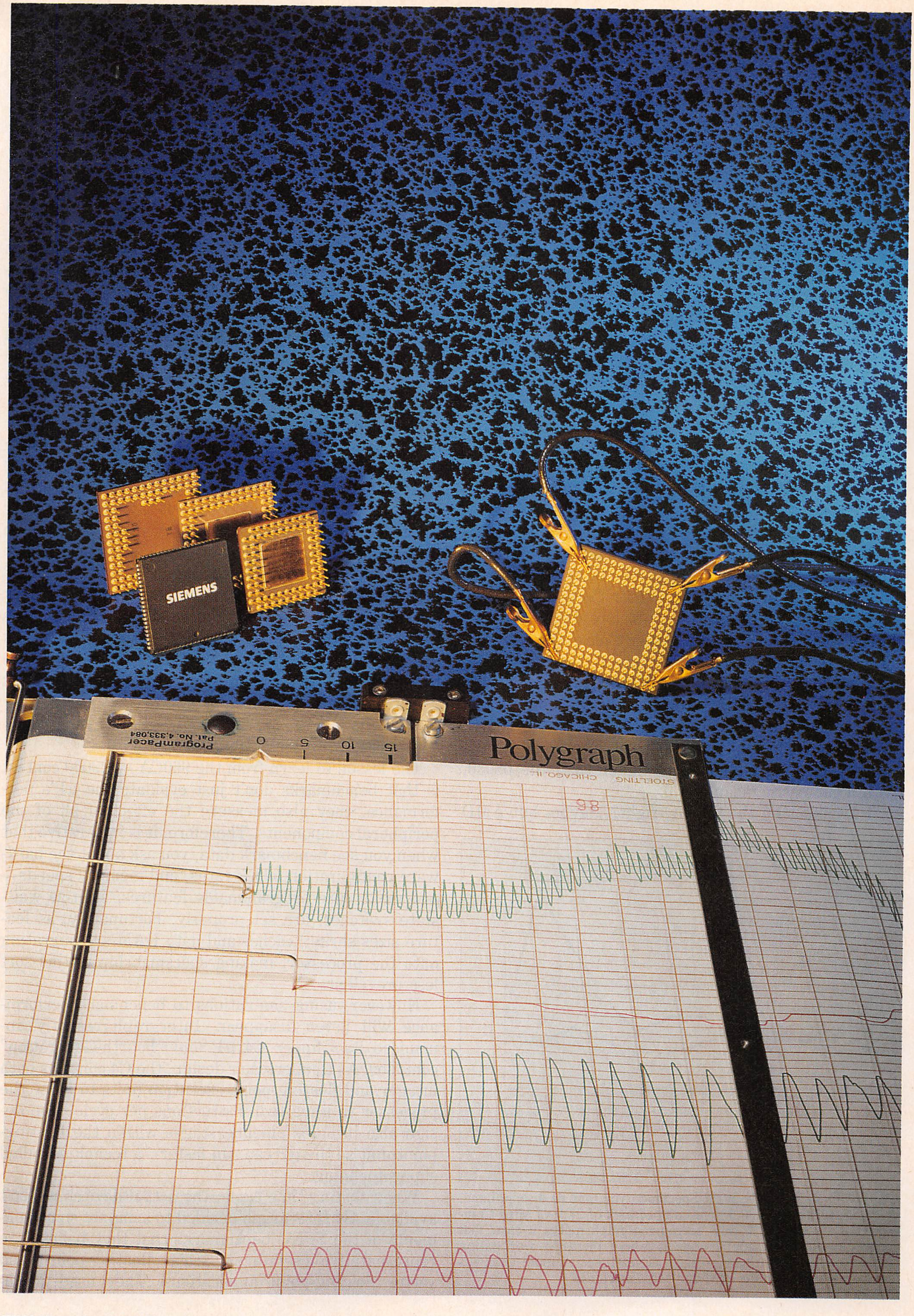
Benchmarks can help you pick from among a multitude of microprocessors and microcontrollers. Unfortunately, to simplify choosing a μP, benchmarks have become a single-number figure of merit for both vendors and designers. This number is—at best—confusing and—at worst—deceiving.

The Systems Performance Evaluation Cooperative (SPEC), a consortium of computer and workstation vendors, was established to develop a suite of consistent and well-defined benchmarks. SPEC has recommended that you not use a single-number figure of merit because it can't provide enough information. Despite SPEC's urgings, users, vendors, and the press have endeavored to make SPEC's 10-benchmark suite more palatable by simplifying the benchmarks into a single figure of merit. In recognition of our tendencies toward simplification, SPEC provided the Specmark (calculated as the geometric mean of the individual benchmark tests) to ensure that the "proper" single number be used—or misused.

Consider the vaunted IBM RS/6000 workstation, powered by IBM's America superscalar microprocessor. (Because IBM isn't making this microprocessor available at the chip level, we've excluded it from our directory.) This μP fetches four instructions at a time from its cache. Under certain circumstances, the processor can dispatch all four instructions in one cycle.

At the workstation roll-out, IBM proudly pointed to a workstation Specmark almost double that of other RISC-processor-powered workstations. Closer inspection of the individual SPEC benchmarks that constitute the Specmark reveals that the IBM workstation's performance is most impressive in two of the floating-point

Although benchmarks can provide useful information, they don't always tell the whole truth. (Photo courtesy Siemens Components Inc)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Remember that what you want from a benchmark and what the vendor wants from a benchmark are not the same.

performance tests. Integer performance, though, is comparable to other RISC workstation benchmarks **(Fig 1)**. IBM uses a floating-point multiply/accumulate instruction to enhance the execution of many floating-point applications.

Supplementing a microprocessor's instruction set with a special-purpose instruction isn't necessarily bad. If the code you are trying to run uses that particular instruction, you'll get higher performance. On the other hand, if you blindly accept a vendor's performance claims, you may end up selecting a processor optimized for operations you'll never use.

Benchmarks can confuse or illuminate

Getting vendors to provide you with multiple benchmark results only eliminates part of the confusion. When Intel announced its 80960CA superscalar, it compared the μP against its own 80960KA, Motorola's 68030, and AMD's 29000 using a suite of nine integer benchmarks (Dhrystone 1.1, Buffer Copy, Annealing, Pi, Quicksort, Bubblesort, Integer Matrix Multiply, CCITT Image Compression, and a Bezier Curve calculation).

Intel reported all results normalized to the 68030. The benchmarks showed the 960CA to be from 2 to 10.8 times faster than the 68030. The geometric mean of all nine benchmark programs indicated the 960CA was 3.9 times faster than the 68030. The 29000 results ranged from 0.4 to 1.7 times faster than the 68030, with a geometric mean of 1.0.

A knockout by the 960CA, right? Maybe, but AMD said the 29000 had both hands tied behind its back. AMD claimed the benchmark was rigged by Intel's choice of the STEB Standalone Evaluation Board. AMD said the board is a low-performance design that supports neither burst-memory accesses nor simultaneous access to instructions and data. Worse, AMD charged that, although Intel replaced the board's 120-nsec memory with the same 35-nsec chips they used in evaluating the 960KA, Intel did not reprogram the board's wait-state switches to take advantage of the 29000 board's faster memory.

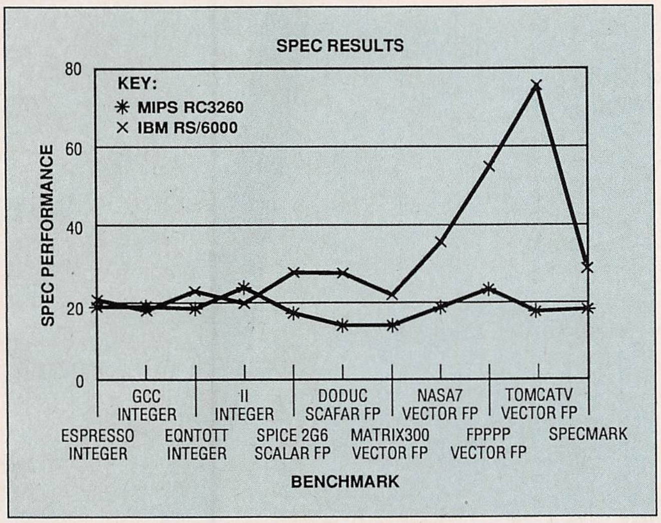

Fig 1—If you look only at the Specmark, you may be disappointed. Whereas IBM's RS6000/530 has a Specmark of 28.9 vs Mips Computers' RC3260's 18.3, this reorganized graph makes it clear that vector-floating-point applications is where the IBM workstation shines. Integer performance—such as you'd see running Unix—is comparable between the IBM and Mips machines.

In response to what they saw as improper benchmarking, AMD requested copies of the individual programs from Intel. AMD then recompiled the code using the current release of its HighC29K C compiler at full optimization. (Intel's report did not say which compiler version it used.) Then the company reran the code on the STEB board, as well as on three high-performance YARC Systems' 29000-based boards. One of the YARC boards ran at 33 MHz and had a data memory of 512k bits of 2-way interleaved 35-nsec static RAM. AMD's testing showed the 33-MHz, 29000-based YARC board was somewhat faster than the 960CA on most of the benchmarks—even though you can't buy a 33-MHz 29000.

Benchmarks measure the whole system

The lesson to learn from the 960CA vs 29000 contest is that benchmarks don't just evaluate the μP's performance, they also measure the effect of all of the peripheral components. Therefore, it is imperative that when you see benchmark data, you ask about the hardware configuration, clock rates, and memory speeds—and make sure programmable features, such as wait-state switches, are set properly. Fortunately, as feature sizes shrink, caches and data RAM are migrating onto the processor, making specsmanship of this sort less prevalent.

However, using simulations to benchmark performance will never disappear. Intergraph recently announced its Clipper C4 μP and "Fourth-Generation" compiler. As a superscalar design, the C4 contains both integer and floating-point execution units to allow the processor to issue two instructions per cycle. The design also includes pipeline stages within the floating-point unit so the μP can run faster—a technique called superpipelining.

When testing time came, the actual devices weren't available. So Intergraph decided to simulate small segments of the SPEC benchmarks that they believe are representative of integer, scalar floating-point, and vector floating-point applications. They used 23 instructions from the Espresso routine for the integer benchmark. The scalar floating-point benchmark was composed of 21 instructions from the Spice program. To measure vector floating-point performance, they used 34 instructions from the inner loop of the Linpack benchmark.

Running on the C4 software model at 50 MHz, these snippets of simulated code allow Intergraph to claim a peak performance of 94 MIPS and 33.3M floating-point operations per second (flops) by executing 1.88 Linpack-inner-loop instructions per clock. Better still, the company uses these results to compare performance to two other theoretical machines: a pure superpipelined and a pure superscalar machine. To achieve 94 MIPS and 33.3M flops performance, a "pure superpipelined machine" that executes 1 instruction per cycle would have to run at 94 MHz. Alternatively, a "pure superscalar machine" running at 25 MHz would have to execute 3.7 Linpack-inner-loop instructions per clock. While all this sounds pretty impressive, you must remember whence these numbers originate.

The C4 example demonstrates that small benchmarks are even easier to manipulate than large ones. Dhrystone is a small standard benchmark that has been abused almost to the point of being meaningless. Rumors abound about compilers that sense Dhrystone source code and output canned, hand-optimized executable programs. Since the Dhrystone benchmark is small, it also fits neatly into a 16k-byte cache, eliminating time-consuming cache misses. And, the Dhrystone benchmark spends 30 to 35% of its run time doing string copies and string compares, often ignoring the results. Therefore, compilers that sense when computation results aren't subsequently used can skip instructions and grossly skew benchmarks.

Software improves hardware performance

Tuning optimizing compilers is fair game. If a vendor finds execution bottlenecks and adjusts his compilers, obviously the benchmark code will execute faster. These optimization decisions may be at the expense of typical code, however. For example, vendors can rewrite run-time libraries with the Dhrystone character-string manipulation in mind. Then, they adjust the optimizing-routine selection instructions to favor benchmarking code.

SPEC's 10 benchmarks come close to being a "good" set. But even these benchmarks, developed by representatives from many system and workstation vendors, are imperfect. First, they are system benchmarks. Any extrapolation to any one component—microprocessor included—is dangerous.

Second, the SPEC benchmarks were selected and written to eliminate caching the program in fast memory. These benchmarks were larger than 32k bytes because, at the time they were selected, system caches were smaller than 32k bytes. Today, there are systems with 512k-byte caches. If your programs are larger than 512k bytes, the SPEC benchmark results may not represent the performance you are likely to see with your code.

Third, because the SPEC benchmarks only measure CPU and memory performance, they ignore I/O, graphics, and multitasking. Some embedded applications have little use for these features, but other applications might be I/O- or graphics-bound—and the wrong time to find out is after you've committed your design.

Fourth, SPEC wanted to provide a portable and

Index to μP and μC chips in EDN's seventeenth annual directory

Application areas	Page	μPμC
8 bit	97	COP800
	98	PIC 165X family
	99	8048 family
	100	8051/8052 family
	107	TMS370 family
	108	6804/6805
	111	6801/6301/68HC11
	112	6500/1, 65C124, 65C265, 50740, 37700
	115	Z8, Super8
	116	7000 family
	119	8085AH/80C85
	120	Z80
	123	Z180/HD64180
	124	6800/6802, 6809/6309
	127	650X/65C0X
	128	8086/8088
	130	Z280
16 bit	132	H8 family
	134	78K series
	136	65C816/65C802
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	142	80286
	147	MCS-96 family
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	151	80C166
	152	RTX 2000
32 bit	155	Transputer family
	156	Z8000, Z16C00
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	162	340X0 graphics μP family
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	166	1Series 32000
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	170	80386
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	183	R2000/R3000 family
	184	29000 family
	187	88000
	188	80960
	190	i860

If possible, get the vendors to benchmark all or part of your application code.

freely distributable set of benchmarks to the market quickly. There was fast agreement among the members that a Spice simulation offered a useful, universal measure of scalar floating-point performance. However, according to John Mashey, Vice President of Systems Technology at Mips Computer Systems and SPEC committee member, the Spice input deck included in the benchmark suite was supplied by Hewlett-Packard and

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wasn't examined by the organization. Mashey laments that this Spice deck isn't as floating-point intensive as a typical Spice run.

Finally, the last problem with the SPEC benchmarks—indeed with any benchmarks—is that as the computers and systems get more powerful, the benchmarks take less and less time to run. Eventually, the time measurements of each program vanish into the

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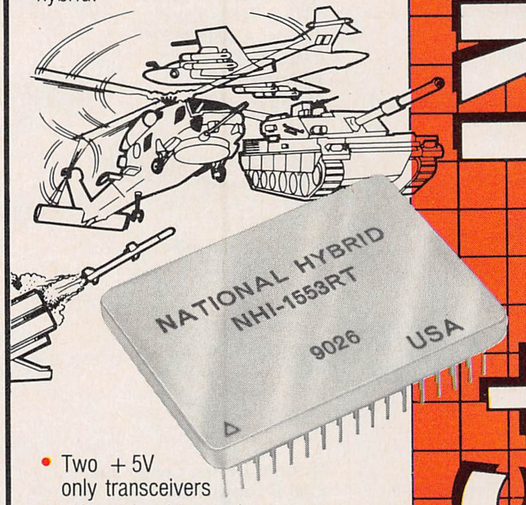

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noise of the system. Whereas the total reference run time on the VAX-11/780 was almost 19 hours, IBM's RS6000 ran the timed portion of the benchmarks in just over 39 minutes.

SPEC's next software revision will push the capabilities of the coming generation of systems. The organization also hopes to include benchmarks to measure I/O performance. Of course, revising its benchmarks will just provide a new target for the microprocessor and system vendors. And, vendors might try to play the old-revision game (use old-revision results if they are more favorable to your goals). As difficult as it may be, SPEC should attempt to move the targets far enough out that it might take four or five generations of systems to make the benchmarks obsolete.

As with many consumables, let the buyer beware. Manufacturers can get benchmarks to say anything they want. General Motors could claim their cars get 60 miles per gallon—by letting the engine idle and rolling the car down a long hill. Fortunately, the Environmental Protection Agency acts as an independent watchdog, performing uniform tests to ensure consistency. The engineering community has no such *independent* watchdog. SPEC, chartered to develop consistent tests, is largely a case of the fox guarding the chicken coop.

Mashey disagrees with that characterization of SPEC. Rather, he sees a bunch of foxes guarding one chicken—each wanting to make sure the other foxes don't get his dinner. SPEC is a consortium composed largely of vendors. It doesn't have to be that way. You can and should get involved in creating the benchmarks and monitoring the results by contacting SPEC, c/o Waterside Associates, 39510 Paseo Padre Pkwy, Suite 350, Fremont, CA 94358. (415) 792-2901. **EDN**

References

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Acknowledgment

We'd like to thank Michael Slater, whose valuable biweekly newsletter, the Microprocessor Report (Sebastopol, CA, (707) 823-4004) provided the inspiration and some of the information for this article.

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Status: Having gained one of the leadership positions in the 4-bit microcontroller field with its COP400 and 16-bit HPC, National introduced this 8-bit controller to fill the gap between those two devices. The architecture of the core µP seems quite simple—a bit like the Motorola 6805. The core-based parts, built on National's double-metal process, are shrinkable to submicron levels.

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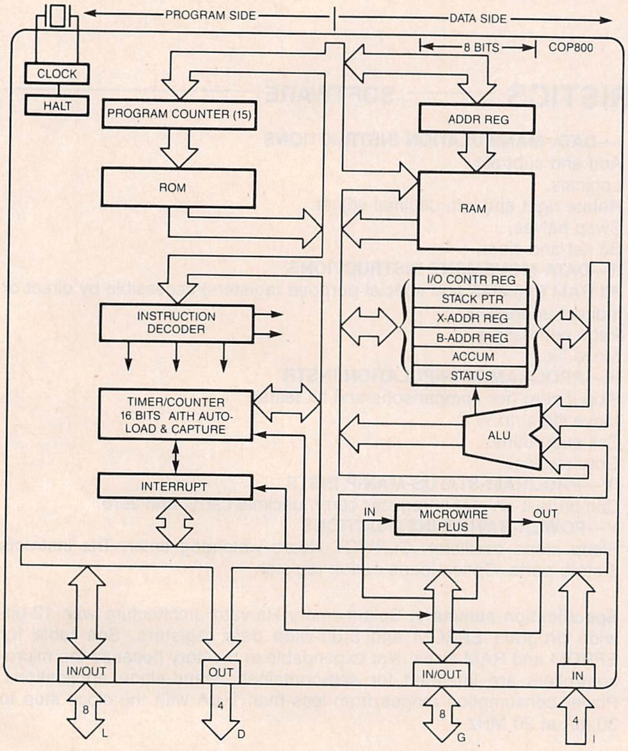


Industrial version (−40 to +85°C)	ROM/EPROM/ EEPROM (bytes)	RAM (bytes)	I/O pins	Interrupt	Timer base counters	Size (pins)	Other
COP820C	1.0k	64	24	3 sources	1	28	
COP821C	1.0k	64	20	3 sources	1	24	
COP822C	1.0k	64	16	3 sources	1	20	
COP8640	2.0k	64	24	3 sources	1	28	64×8-bit EEPROM in RAM
COP8641	2.0k	64	20	3 sources	1	24	
COP8642	2.0k	64	16	3 sources	1	20	
COP8620	1.0k	64	24	3 sources	1	28	64×8-bit EEPROM in RAM
COP8621	1.0k	64	20	3 sources	1	24	
COP8622	1.0k	64	16	3 sources	1	20	
COP8720C	1.0k EEPROM	64	24	3 sources	1	28	64×8-bit EEPROM in RAM
COP8721C	1.0k EEPROM	64	20	3 sources	1	24	64×8-bit EEPROM in RAM
COP8722C	1.0k EEPROM	64	16	3 sources	1	20	64×8-bit EEPROM in RAM
COP840C	2.0k	128	24	3 sources	1	28	
COP841C	2.0k	128	20	3 sources	1	24	
COP842C	2.0k	128	16	3 sources	1	20	
COP880C	4.0k	128	36	3 sources	1	40/44	
COP881C	4.0k	128	24	3 sources	1	28	
COP8780C*	4.0k EPROM	128	36	3 sources	1	40/44	EPROM & OTP
COP8781C*	4.0k EPROM	128	24	3 sources	1	28	
COP884CF	4.0k	128	21	10 sources	2	28	2 PWM & A/D
COP884CG	4.0k	192	23	12 sources	3	28	3 PWM & UART
COP884CL	4.0k	128	23	10 sources	2	28	2 PWM
COP884CS*	4.0k	192	23	12 sources	1	28	1 PWM & UART
COP888CF	4.0k	128	33/37	10 sources	2	40/44	2 PWM & A/D
COP888CG	4.0k	192	35/39	14 sources	3	40/44	3 PWM & UART
COP888CL	4.0k	128	33/39	10 sources	2	40/44	2 PWM
COP888CS*	4.0k	192	35/39	14 sources	1	40/44	1 PWM & UART
COP888EG*	8k	256	35/39	14 sources	3	40/44	3 PWM & UART
COP884EG*	8k	256	23	12 sources	3	28	3 PWM & UART

*Available in 1990
All devices implement their stacks in RAM and have at least 1 serial I/O port.
MIL temperature range available

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, and subtract with borrow.
Logicals include rotates, shift compares, and conditionals.
Decimal correct.
Increment and decrement.
Bit manipulation: set, reset, and test individual bits in data memory, which includes those in data registers and I/O ports.

II—DATA-MOVEMENT INSTRUCTIONS
Load and exchange instructions with optional automatic post increment or decrement of the associated pointer. Most allow the use of either the B or X pointer. Decrement register and skip if zero.

III—PROGRAM-MANIPULATION INSTR
Jump instructions: relative, absolute, absolute long, and indirect.
Subroutine, subroutine long, return, and skip (only the amount of available RAM limits subroutine levels).
Push and pop.

IV—PROGRAM-STATUS-MANIP INSTR
ALU-driven decision bits in status register (PSW) appear to be limited to carry and half-carry flags. These, as well as interrupt control bits for various on- and off-chip interrupt sources, can be set and reset.

V—POWER-SAVING INSTRUCTIONS
Halt mode, which is entered by setting data bit and exited by reset or low-to-high transition on the CKO pin.

Note:
1. Program-branch decisions are implemented in skip-the-next-instruction manner.

Specification summary: 15-bit program counter (PC) can address 32-byte program memory, which can include data and data tables. All data, control, and I/O registers are mapped into data-side memory space. Two bidirectional 8-bit and two unidirectional 4-bit I/O ports max. Each I/O pin has software-selectable options to adapt the chip to specific applications. On-chip peripheral functions include software-selectable I/O of as many as 39 I/O pins, 3-wire serial I/O, 16-bit timer/counter with capture register and auto reload, and an 8-source interrupt. Maximum speed is 1-µsec instruction cycle (most instructions take one cycle). Clock for 1-µsec cycle is 10 MHz. Operates over 2.5 to 6V range and draws 9 mA running full speed at 1-µsec cycles, but less than 1 µA when halted.

Hardware notes:
1. Diagram shows basic COP800-family architecture. Each member of growing family has an emulator part that replaces standard masked-ROM with EEPROM or EPROM.
2. Sierra says cost of ASIC design can be as low as $40,000 up front (16 weeks' time), meaning ASICs can be cost competitive for 100k quantities.

HARDWARE — SUPPORT — SOFTWARE

Supported on National COP800 Development Systems. The system can be used in conjunction with IBM PC as host. Applications Hot Line: (408) 721-5582.

Cross-assembler for IBM PC and other computers. Form-fit emulators are available for every member of the family. These parts are 2-chip hybrids or single-chip EPROMs or EEPROMs.

PIC 16C5X FAMILY

8-BIT CMOS

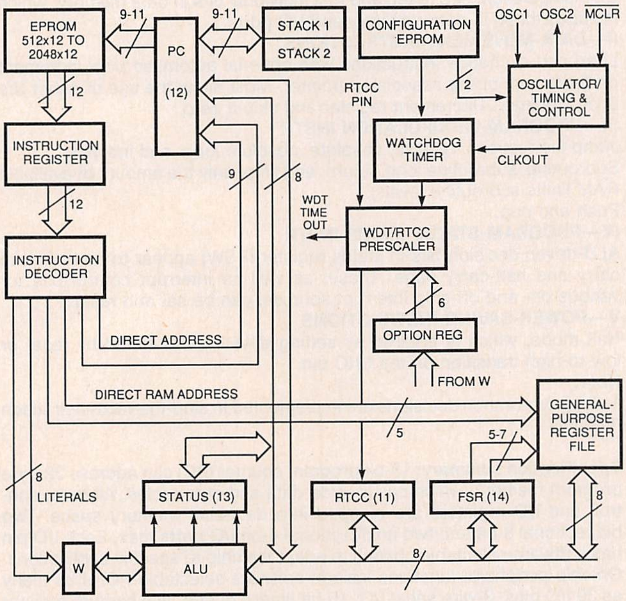
AVAILABILITY: Now.
COST: Under $1.50 in volume.
SECOND SOURCE: None.

Description: A family of single-chip CMOS EPROM-based microcontrollers that use only 33 single-cycle/single-word instructions. The family offers various amounts of I/O, RAM, and one-time programmable EPROM. Oscillator frequency ranges from dc to 20 MHz. Although it qualifies for the RISC moniker based on its 33 instructions, using the label to describe it is risky, if not confusing. The family only has a 2-stage pipeline without delayed branches or load delay slots rather than a 4- or 5-stage pipeline with delayed branches and load delay slots. The chips have a 2-address instruction format rather than the 3-address instruction format typical of RISC machines. Also, the PIC family must be programmed in assembly language—there are no compilers.

Microchip Technology Inc
2355 W Chandler Blvd
Chandler, AZ 85224
Phone (602) 963-7373
For more information, Circle No. 352

Status: To date, 75 million PICs have been sold worldwide, generally in high-volume, low-end consumer, personal computer, and automotive applications. CMOS one-time programmable versions were introduced in 1989 and are embedded in more than 1000 designs.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract.
Logicals.
Rotate right and left, decimal adjust.
Swap halves.
Bit set and clear.
II—DATA-MOVEMENT INSTRUCTIONS
All RAM (general- and special-purpose registers) accessible by direct or indirect addressing.
Page addressing.
Move file.
III—PROGRAM-MANIPULATION INSTR
Skip if zero (for comparisons and bit tests).
Move literal to W.
Call subroutine.
Goto routine.
IV—PROGRAM-STATUS-MANIP INSTR
Can bit test on status-register carry, decimal carry, and zero.
V—POWER-SAVING INSTRUCTIONS
Sleep stops oscillator, CLRWDT clears watchdog timer. Tris instructs 3-state ports. Option loads option register.

Specification summary: Split-memory Harvard architecture with 12-bit-wide program EPROM and 8-bit-wide data registers. See table for EPROM and RAM sizes. Not expandable in memory because the microcontrollers are intended for self-contained, stand-alone applications. Power consumption ranges from less than 1 μA with the clock stop to 30 mA at 20 MHz.

PIC 16C5X CMOS microcontrollers

Part number	Pins	I/O	RAM (bits)	EPROM (bits)
PIC16C54	18	12	32×8	512×12
PIC16C55	28	20	32×8	512×12
PIC16C56	18	12	32×8	1024×12
PIC16C57	28	20	80×8	2048×12

Hardware notes:
1. 12-bit-wide instruction word allows single-cycle execution of all instructions.
2. All current devices are fully static, silicon-gate CMOS designs that feature an 8-bit real-time-clock counter, watchdog timer, and 2-level program-counter-save stack for subroutine nesting.
3. Security EPROM fuse for user's code protection.
4. A lower-cost RC-oscillator version is also available for applications that aren't timing critical.

HARDWARE — SUPPORT — SOFTWARE

Microchip offers two IBM PC-hosted development systems. One, the Pik-Pak is a low-end development system that allows for assembly, execution, debugging, and analysis of microcode. The $495 price includes programmer and UV-erasable samples. The Pic-ICE development system ($2495) offers full-speed emulation to support real-time code development. The system includes in-circuit emulation pod with an 8k capture-trace buffer, programmer, and diagnostic demo board. High-volume programming support is available from Microchip, Data I/O (Redmond, WA), and Logical Devices (Fort Lauderdale, FL).

Picalc cross-assembler is an IBM PC-hosted software tool that offers full-featured macro and conditional assembly capability. Picsim simulator software allows simulation of the PIC16C5X products on an instruction level. The simulator allows single-step, execute-until-break, and trace modes. Pice emulator software offers an interface with pull-down menus.

8048 FAMILY

8-BIT NMOS AND CMOS

AVAILABILITY: Now.

COST: Masked-ROM parts are less than $2 in high volume (100k). EPROM parts cost $18 (100). CMOS parts cost as little as $3 (100k). Windowless-PROM parts cost $8 (5000).

SECOND SOURCE: Toshiba, NEC, Signetics/Philips, National Semiconductor, Oki, Fujitsu, UMC (Taiwan), with volume spread out among suppliers.

CORE: Zymos has been using 80C49 as a core for ASICs for several years. Others are following because 8048/49 combines popularity with small core size.

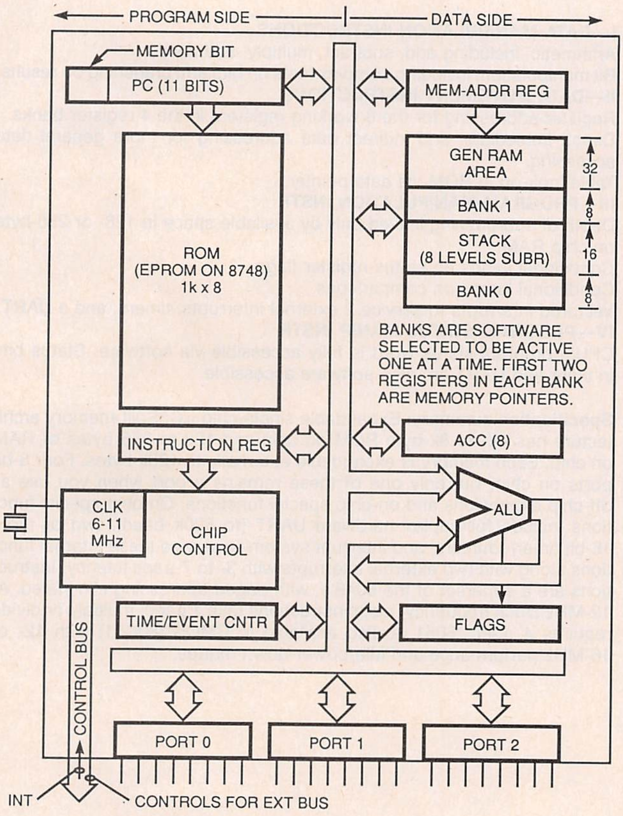
Description: Broad family of single-chip controller-type µCs, including a version that can function as a slave (8041). Basic models don't have serial communications ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 353

Status: Intel is still bullish about the 8048. However, Intel chose the 8051 over the 8048 as the kick-off core for ASICs and says it has no definite plans to use the 8048 as an ASIC core.

CHARACTERISTICS

HARDWARE



Hardware notes:

1. Diagram is for basic 8048. Table indicates some other basic parts, most of which exist in both NMOS and CMOS.
2. CMOS parts are designated 80C48, 80C49, 80C50, etc.
3. There are many other variations of the basic 8048 among the many suppliers. For example, Intel's 8041/42 chips are software compatible but are configurable as slaves to host µPs for interface applications. The National NS 405/455 uses the 8048 core as the basis of a terminal controller. Siemens has the telecommunications-oriented 80C382/482. A number of semicustom houses use the 8048 as a core processor in their libraries.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Bit set and reset.
Two working banks of 8-bit registers.
II—DATA-MOVEMENT INSTRUCTIONS
Both internal and external RAM are fully accessible by instruction set.
Indirect and direct data fetches.
III—PROGRAM-MANIPULATION INSTR
Decrement and skip if zero.
More than 20 conditional branches.
8-level stack with expansion capability.
Two vectored interrupts.
Two programmable flag bits under software control.
IV—PROGRAM-STATUS-MANIP INSTR
Status word is fully accessible and is stored in the stack.

Specification summary: Split-memory architecture with 1k to 4k bytes of program ROM or EPROM on chip and 64 to 256 bytes in separate space, also on chip. I/O has its own space and instructions to operate directly on I/O ports. All spaces are expandable: program memory to 4k bytes, data memory to 256 bytes, I/O to unlimited amounts. I/O can use 8080/85 peripherals. Devices have 8-level stack for subroutine nesting and interrupt response. Dual banks of working registers allow rapid context switching. Family members execute their 1- and 2-cycle instructions at 1-cycle times ranging from 1.36 to 15 µsec. NMOS 5V technology in 40-pin DIP and 44-pad chip carriers; UV-erasable ROMs (EPROMs) and windowless PROM parts are available. CMOS versions available with idle and power-down features and optional flatpack packages. The 8049KB can drive four 10-mA LEDs.

Part no.	Memory (bytes)			Package pins	
	ROM	EPROM	RAM	Parallel I/O	Total
8035	0	0	64	3×8	40
8048	1k	0	64	3×8	40
8748	0	1k	64	3×8	40
8039	0	0	128	3×8	40*
8049	2k	0	128	3×8	40*
8749	0	2k	128	3×8	40*
8040	0	0	128	3×8	40
8050	4k	0	256	3×8	40

*Also available in 44-lead PLCC package.

SUPPORT

HARDWARE

From Intel: Intel plays down 8048 support, saying that there are now numerous third-party OEM suppliers of PC-hosted emulators for the 8048 family.

From NEC: Ekakit 84C-1 stand-alone emulator (less than $2000).

SOFTWARE

From others: Because of the broad-based popularity of this family, dozens of independent sources of development and application software exist, including support on universal development systems from Tektronix (Beaverton, OR) and Applied Microsystems (Redmond, WA).

Program library: Insite Library contains a variety of application programs.

8051/8052 FAMILY

8-BIT NMOS AND CMOS

AVAILABILITY: Now for 8051, 80C51, 8031, 80C31, 8751, 87C51, 80C32, 83C51FA, 87C51FA, 83C51FB, 87C51FB, 8032, 8052, and 87C51FC.

COST: $2.30 (2k) for 8051; $33 (1k) for 8751; $3 (2k) for 80C51; $2.95 (2k) for 8052; $44 (1k) for 87C51; $40 (1k) for 8752; $4.40 (2k) for 80C52; $4.90 (2k) for 83C51FA; $45 (1k) for 87C51FA; $50 (1k) for 87C51FB; and $67 (1k) for 87C51FC.

SECOND SOURCE: Siemens, Signetics/Philips, Fujitsu, Oki, and Harris-Matra (France) licensed.

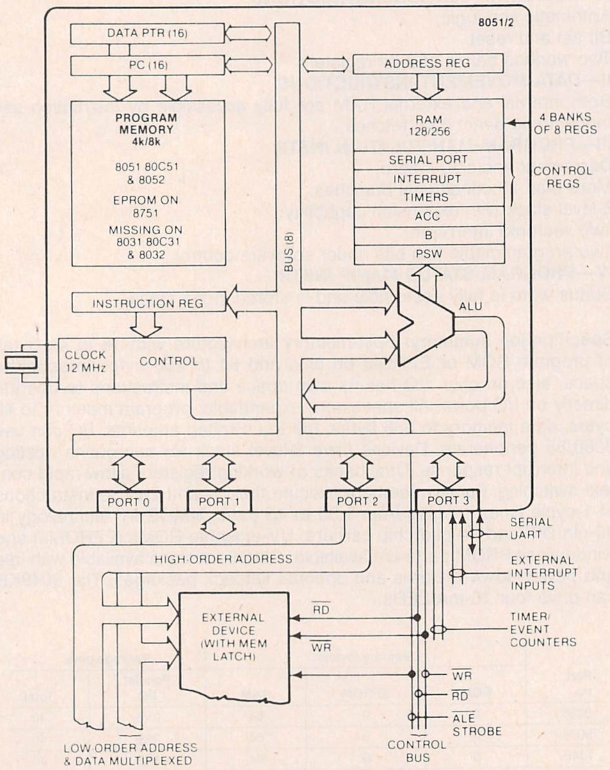
CORE: Intel's ASIC Components Group is using the 8051 as its starting µP core. Signetics/Philips has the 80C51 core in its ASIC library.

Description: Expandable single-chip controller, an enhanced version of the same supplier's widely used 8048 family. Architecturally, it features nonpaged addressing for easier programming; more interrupts with extra RAM-register banks to service them; increased stack depth; and new instructions, such as multiply, divide, and compare.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 354

Status: Generally thought of as the leader among the more powerful 8-bit single-chip µCs. This family faces stiff competition from high-end 8-bit µCs, such as Mitsubishi's 50740 version of the 6500/1, Motorola's 68HC11, NEC's 7811, Hitachi's 647180, and National's COP800, as well as from 16-bit µCs, such as Intel's own 8096 and National's 16040. The 8051 is among the most widely used cores in market-specific µCs.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The 14 members of the 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip ROM.
2. The 8051's Boolean-processor capabilities refer to the way instructions can single out bits in RAM, accumulators, I/O registers; perform complex bit tests and comparisons; then execute relative jumps based on results.
3. Intel has one 8052 model preprogrammed with a full Basic interpreter.
4. Dallas Semiconductor (Dallas, TX) offers an 8051-instruction-code-compatible µP ($9.70 (1000)), which converts as much as 64k bytes of SRAM into lithium-backed nonvolatile memory. The chip also provides a serial bootstrap loader for initialization, crashproofing circuitry to save current state, and on-chip software encryption that loads and executes the application in unintelligible form.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, multiply, and divide.
Bit manipulation, including complex tests on bits and branching on results.
II—DATA-MOVEMENT INSTRUCTIONS
Register addressing for the 8 working registers in the 4 register banks.
Direct, immediate, and indirect data addressing for more general data accessing.
Table look-up in ROM via data pointer.
III—PROGRAM-MANIPULATION INSTR
Depth of subroutining limited only by available space in 128- or 256-byte on-chip RAM.
Conditional jumps on status-register flags.
Conditional jumps on comparisons.
Vectored interrupts to service 2 external interrupts, timers, and a UART.
IV—PROGRAM-STATUS-MANIP INSTR
CPU's program-status word is fully accessible via software. Status bits in timer and UART are also software accessible.

Specification summary: Expandable single-chip µC. Split-memory architecture has 4k- to 8k-byte ROM on chip and 128 to 256 bytes of RAM on chip. Each memory is expandable externally to 128k bytes. Four 8-bit ports on chip, but only one of these remains a port when you use all off-chip expansions and on-chip special functions. On-chip special functions include full-duplex hardware UART (to 500k baud), two or three 16-bit timer/counters, and interrupt system to service these internal functions along with two external interrupts with 3- to 7-µsec latency. Instructions are a superset of the 8048's, with paged addressing eliminated. At 12-MHz clock frequency, most instructions take 1 µsec; multiply or divide requires 4 µsec. 8051 is also available in CMOS (80C51) with 12- or 16-MHz performance and idle/power-down modes.

HARDWARE — SUPPORT — SOFTWARE

From Intel: ICE-5100/252 in-circuit emulator ($5495) supports the entire MCS-51 family including 8051, 8052, and 80C52. Comes with macroassembler and editor. IBM PC/AT/XT, running DOS 3.1 or later versions, and Intellec Series III/IV development systems host the emulator. Nohau (Campbell, CA) and MetaLink (Chandler, AZ) provide PC-hosted emulation systems for Signetics/Philips standard and derivative µCs.

From Intel: ASM-51 and PL/M-51, both containing a relocation and linkage utility, are available for the IBM PC and Intel microcomputer development systems.
From others: Many third-party software suppliers offer C compilers for 8051 with special features suited to microcontroller applications. Three such compilers are Micro Computer Control's (Hopewell, NJ) for $1495, Archimedes Software's (San Francisco, CA) for $851, and Franklin Software Inc's (San Jose, CA) for $895. All are hosted on IBM PC.

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When You Need Fast Cache.

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Part No.	Organization	Access Time ns	Package (all 28-pin)
M5M5178A	8K x 8	15, 20, 25	SOJ, Flat Pack, DIP
M5M5179A	8K x 9	15, 20, 25	SOJ, Flat Pack, DIP
M5M5180A	8K x 8 (Latched)	20, 25	SOJ, Flat Pack, DIP

Mitsubishi's fast SRAMs let you cash in on your cache subsystem performance. Just match memory density and organization with any of the popular industry-standard microprocessors. You get the speed you need, and use fewer components. In fact, with its on-chip address latch, the M5M5180A can reduce chip count by as much as 50% in an 8K x 32 cache memory subsystem.

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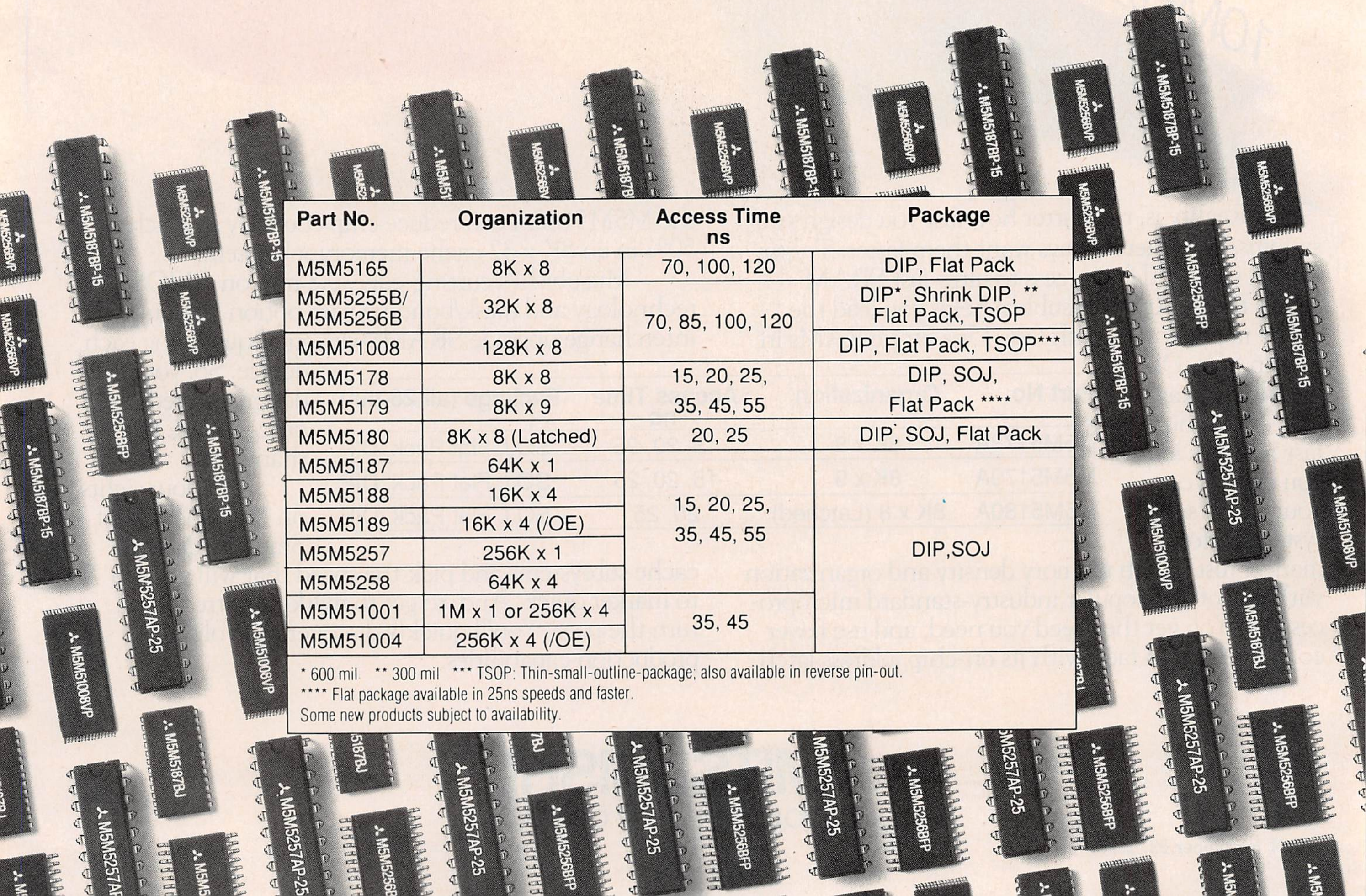

Part No.	Organization	Access Time ns	Package
M5M5165	8K x 8	70, 100, 120	DIP, Flat Pack
M5M5255B/ M5M5256B	32K x 8	70, 85, 100, 120	DIP*, Shrink DIP, ** Flat Pack, TSOP
M5M51008	128K x 8		DIP, Flat Pack, TSOP***
M5M5178	8K x 8	15, 20, 25, 35, 45, 55	DIP, SOJ, Flat Pack ****
M5M5179	8K x 9		
M5M5180	8K x 8 (Latched)	20, 25	DIP, SOJ, Flat Pack
M5M5187	64K x 1	15, 20, 25, 35, 45, 55	DIP,SOJ
M5M5188	16K x 4		
M5M5189	16K x 4 (/OE)		
M5M5257	256K x 1		
M5M5258	64K x 4		
M5M51001	1M x 1 or 256K x 4	35, 45	
M5M51004	256K x 4 (/OE)		

* 600 mil ** 300 mil *** TSOP: Thin-small-outline-package; also available in reverse pin-out.
**** Flat package available in 25ns speeds and faster.
Some new products subject to availability.

When you need less.

When you need to pack more memory in less space and reduce power, Mitsubishi offers standard and soon, fast SRAMs in TSOP (thin-small-outline packaging). Static RAM packaging can't get any smaller than the TSOP, since it's virtually the size of the die.

Our TSOP SRAMs take up only half the surface area and are four times smaller in volume than equivalent pin-count, standard surface-mount packages. And, with a profile half that of standard surface-mount packages (1.2mm) and a low standby current (20μA to 50μA), TSOPs are perfect for portable, handheld, battery-backed applications.

So, if your design requires a lot of static RAM or just a little, call Mitsubishi for some action. We'll bring your vision to reality. Mitsubishi Electronics America, Inc., Electronic Device Group, 1050 E. Arques Ave., Sunnyvale, CA 94086. 1-800-624-8999 ext. 178C.

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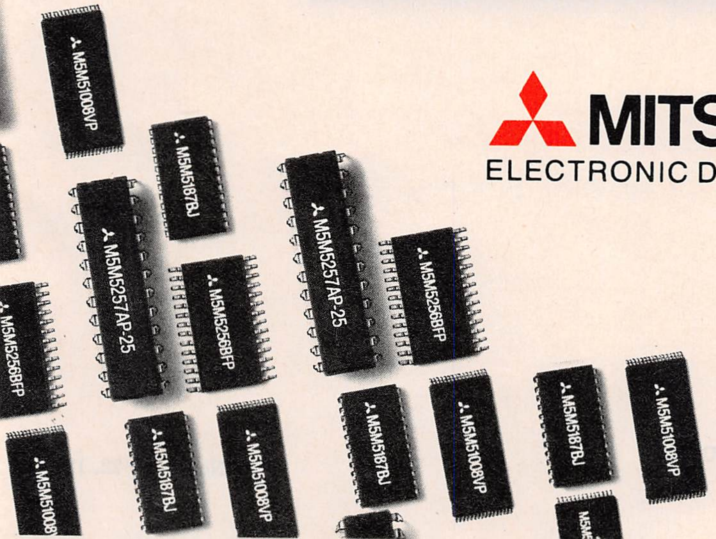
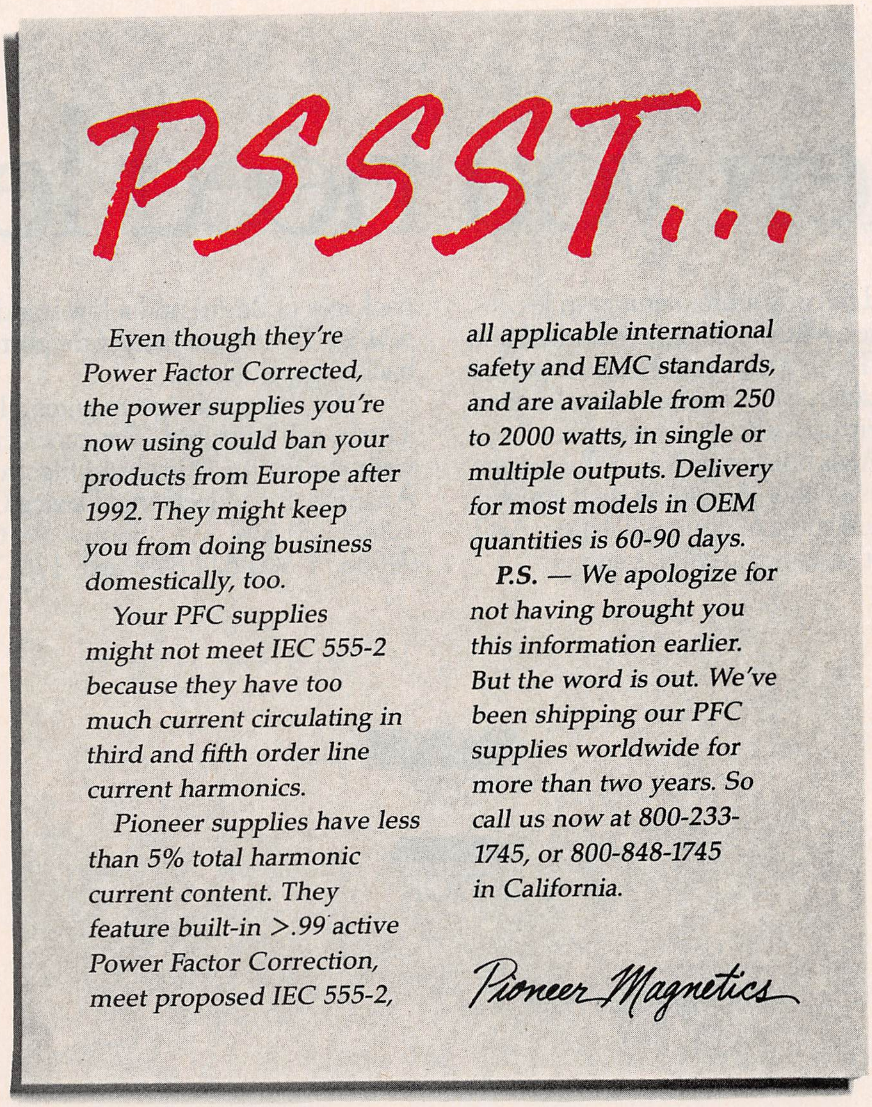
TSOP



MITSUBISHI
ELECTRONIC DEVICE GROUP

CIRCLE NO. 103



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Pioneer Magnetics

CIRCLE NO. 114

TMS370 FAMILY

8-BIT CMOS

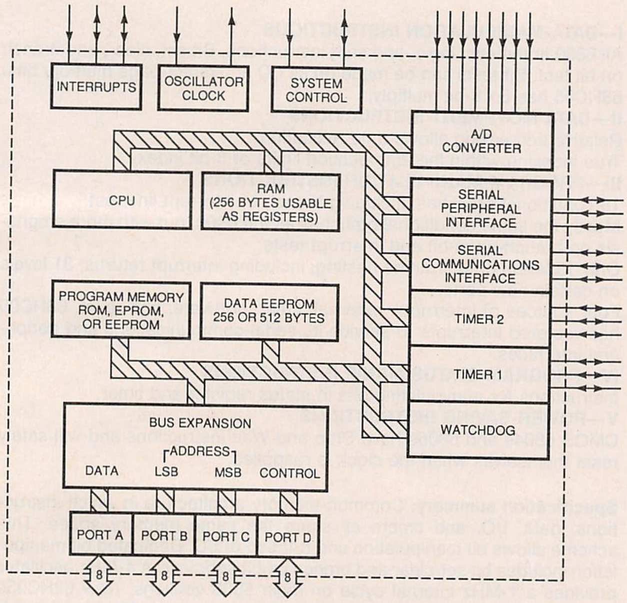
AVAILABILITY: Now.
COST: ROM-based devices range from $3.50 to $11 (100k) depending on program memory, peripherals, and on-chip EEPROM mix.
SECOND SOURCE: None.

Description: Software-compatible family of CMOS μCs with on-chip EEPROM and peripheral support functions. Modular design architecture provides flexible reconfiguration and reduction in product design time. Various family members incorporate an 8-channel, 8-bit A/D converter, enhanced timers, serial peripheral interface, serial communications interface, EPROM, EEPROM, and ROM. Instructions typically perform combined load, operation, and store functions, increasing system performance and code efficiency. Form-factor emulator versions replace ROM with EPROM or EEPROM and allow prototyping and small runs.

Texas Instruments Inc
Microprocessor and Microcontroller Products Div
Box 809066
Dallas, TX 75380
Phone (800) 232-3200
For more information, Circle No. 355

Status: Supports real-time applications that may previously have required analog, bit-slice, or multiple controllers. The alterable nonvolatile memory allows the μC to retain critical data without power. The vendor offers 16 function modules that it will configure for your application if your volumes exceed 50,000.

HARDWARE — CHARACTERISTICS — SOFTWARE


INTERRUPTS
OSCILLATOR CLOCK
SYSTEM CONTROL
A/D CONVERTER
CPU
RAM (256 BYTES USABLE AS REGISTERS)
SERIAL PERIPHERAL INTERFACE
SERIAL COMMUNICATIONS INTERFACE
PROGRAM MEMORY ROM, EPROM, OR EEPROM
DATA EEPROM 256 OR 512 BYTES
TIMER 2
TIMER 1
BUS EXPANSION
ADDRESS
DATA
LSB
MSB
CONTROL
WATCHDOG
PORT A
PORT B
PORT C
PORT D
8
8
8
8

Hardware note:
Diagram reflects the TMS370x5x, which supplements the 370Cx1x's single 16-bit timer, serial peripheral interface, programmable timer, 128-bit SRAM, and optional 256-bit EEPROM with a second 16-bit timer, a serial communications interface, memory expansion ports, another 128 bits of SRAM, and an 8-channel 8-bit ADC. The 370Cx3x contains a programmable timing module with watchdog timer, a miniserial communications interface, an 8-channel 8-bit ADC, 256-bit SRAM, and optional EEPROM.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8×8-bit multiply, 16×8-bit divide, and BCD.
Logicals, increment, and decrement.
Rotates right and left. Bit test. Set bit.
II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Apply to many instructions.
Indexing via B register.
16-bit moves.
III—PROGRAM-MANIPULATION INSTR
Call and return. Trap. Bit test and jump on both I/O and memory. Conditional jumps using program-counter-relative addressing.
IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, overflow, and interrupt enable.
Instructions to change carry and interrupt enable.

Specification summary: The programmable timer module uses the on-chip dual-ported RAM to store its commands as well as the timer values. This module allows input capture on as many as 6 pins, 4 of which have a programmable prescaler. The TMS370 CMOS family members use a 5V supply over the oscillator frequency range of 2 to 20 MHz and over the temperature range of -40 to +85°C. The application program, register file, and peripheral file share memory space.

TMS370 family matrix

	370C×C	370C×32	370C×50	370C×52	370C×56
ROM	4k	8k	4k	8k	16k
FFE	4k EEPROM	8k EEPROM	4k EEPROM	16k EPROM	16k EPROM
Data EEPROM	256	256	256	256	512
RAM	128	256	256	256	512
Timer 1, watchdog timer	●		●	●	●
Timer 2			●	●	●
Serial peripheral interface	●		●	●	●
Serial communications interface		●	●	●	●
A/D port		●	●	●	●
I/O links	22	55	55	55	55
Package	28 DIP/PLCC	68 PLCC	68 PLCC	68 PLCC	68 PLCC

HARDWARE — SUPPORT — SOFTWARE

From TI: XDS/11 is a IBM-PC-driven interactive development system ($2850). It provides full-speed, in-circuit emulation and debugging functions. XDS/22 development system ($8250) adds extended breakpoint, trace, and timing functions to the XDS/11 system. A design kit ($370) lets you analyze the feasibility of using the TMS370 family for your application. EEPROM programmer ($1250) comes with power and interface cables, software, and sockets for the 370 family and EPROMs such as the 2732, 2764, 27128, and 27256.
From others: ElectroRent provides rental use of TI tools for IBM PCs. Logical Devices (Fort Lauderdale, FL) has a TMS370 microcontroller module for AllPro programmers.

From TI: Cross-assembler, linker, full ANSI C compiler, and C source debugger available on IBM PCs and DEC VAXs under VMS.
From others: Allen Ashley (Pasadena, CA) supplies an assembler/linker and Intermetrics (Cambridge, MA) offers a C compiler that runs on IBM PCs. Macrochip Research (Carrollton, TX) has an assembler and midrange emulator for both IBM and Macintosh personal computers. P&E Microcomputer Systems (Woburn, MA) provides an integrated assembler and simulator for IBM PCs.

6804/6805

8-BIT NMOS AND CMOS

AVAILABILITY: Now for most models. Motorola can build customer-specified versions in as little as six months.

COST: $1 to $8. CMOS parts are more expensive than NMOS ones.

SECOND SOURCE: Harris, Hitachi, and SGS Thomson.

CORE: Motorola and NCR have a joint ASIC pact to use CMOS 6805 as a core along with NCR's similar 6502 µP core. SGS Thomson has ST6 core, which has architecture somewhat similar to the 6804's.

Description: Family of single-chip µCs based loosely on 6800 architecture but in some ways more like 6502 (especially 6805). Family offers various amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 4 MHz. Some parts contain an on-chip A/D converter, EEPROM, serial I/O, and software security. Customer-specified microcontrollers use this core for mixing and matching of peripherals to reduce cost for specific customer applications.

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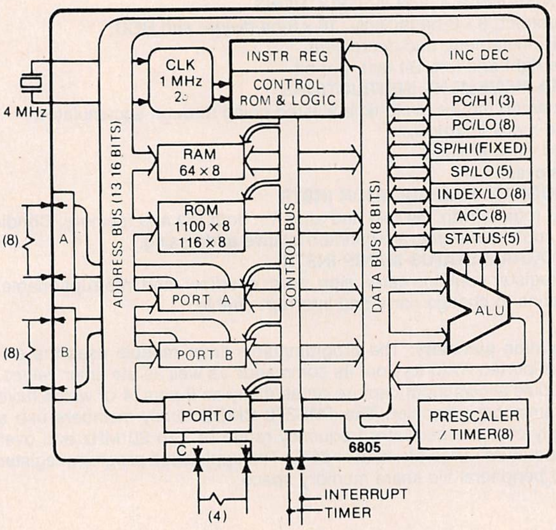
Status: Supplier's steady commitment to this family over past 12 years has paid off. It trails only the 8048/49 family and the 50740 in market share. Motorola continues to expand the 6805 family, using its CSIC (customer-specified integrated circuit) concept.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test. Bit tests can be made on all I/O and direct-page memory bits. 68HC05 has 8 × 8-bit multiply.

II—DATA-MOVEMENT INSTRUCTIONS
Relative addressing allows data relocation.
True indexing within the 256-location limits of 8-bit index.

III—PROGRAM-MANIPULATION INSTRUCTIONS
18 conditional branches, including branch of interrupt line test.
Mostly the same conditional branches as the 6800, but with more emphasis on branch-upon-bit and interrupt tests.
Only 15 levels of subroutine nesting, including interrupt returns; 31 levels on certain new parts.
Four sources of interrupts: external, timer, software, and reset. 68HC05 has vectored interrupts to service its serial-communications and peripheral interfaces.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Instructions for manipulating bits in status register and timer.

V—POWER-SAVING INSTRUCTIONS
CMOS 6804s and 6805s have Stop and Wait instructions and will safely reset themselves when the clock is reapplied.

Specification summary: Common-memory architecture in which instructions, data, I/O, and timers all share the same memory space. This scheme allows bit manipulation and rotation of I/O. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most 6805 versions. New 68HC05s have a 2.1-MHz internal bus speed. Some, like the 68HC705C8, are available with a 4-MHz bus speed. Some parts offer program security, on-chip 5V EEPROM, A/D converter, serial peripheral interface, serial communications interface, timers, PWM D/A converter, LCD drivers, DTMF generators, and other customer-specified peripherals. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs, SOICs, and shrink DIPs; 44-, 52-, and 68-pin PLCCs; and other fine-pitch packaging options.

Family		Speed bus (MHz)	Instructions	On-chip ROM	RAM	I/O pins	Timer	Interrupts	Power consumption (mW)	Pins
6805	Min	0	51	1k	64	16	—	3	0.01	28
	Max	2	59	4k	176	32	Yes	5	–700	40
68HC05	Min	0	62	1k	96	32	Yes	2	0.25	40
	Max	4	62	16k	304	32	Yes	2	0.25	68

Hardware notes:

1. Diagram is for nonexpandable Model P2 in a 28-pin package.
2. Comparison of 6805 with 6800: Stack is only 64 bytes deep. Only one accumulator. Index register can only span 256 memory locations. However, family supports a 16-bit offset addressing mode, thus the µP can access 256-byte tables anywhere within the memory space. Program counter is as long as 14 bits in some members of this family. Only one external interrupt is provided, but some models have timer-input capture pins, which may provide additional edge-triggered inputs.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Special pin initiates program.
4. Harris has ROMless emulator versions (68EM05/C4,D2) for prototyping and low-volume production. Harris brings all ROM access buses out for direct interfacing to industry-standard EPROMs. Available in 40-pin piggyback for 2764.
5. Motorola currently has five field-programmable 68HC05 versions with on-chip EPROM instead of mask ROM to permit development and low-volume production.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: The less costly M68705EVM (HMOS) and M68HC05EVM (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.
From Harris: Single-board evaluation kit that interfaces to IBM PC via RS-232C line.
From SGS Thomson: INICE4-8 development and emulation system.
From others: A number of third-party companies, including Sophia Systems (Santa Clara, CA) and American Automation (Tustin, CA), provide hardware emulators for the 6805 family. Most of these emulators interface to IBM PCs.

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733.
From SGS Thomson: Interactive development software.
From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has cross-assemblers for 6805 and 6804 that run on IBM PCs and compatibles. Introl (Milwaukee, WI) provides cross-compilers and cross-assemblers. C cross-compiler with macro cross-assembler from Bytecraft Ltd (Waterloo, Ontario, Canada).

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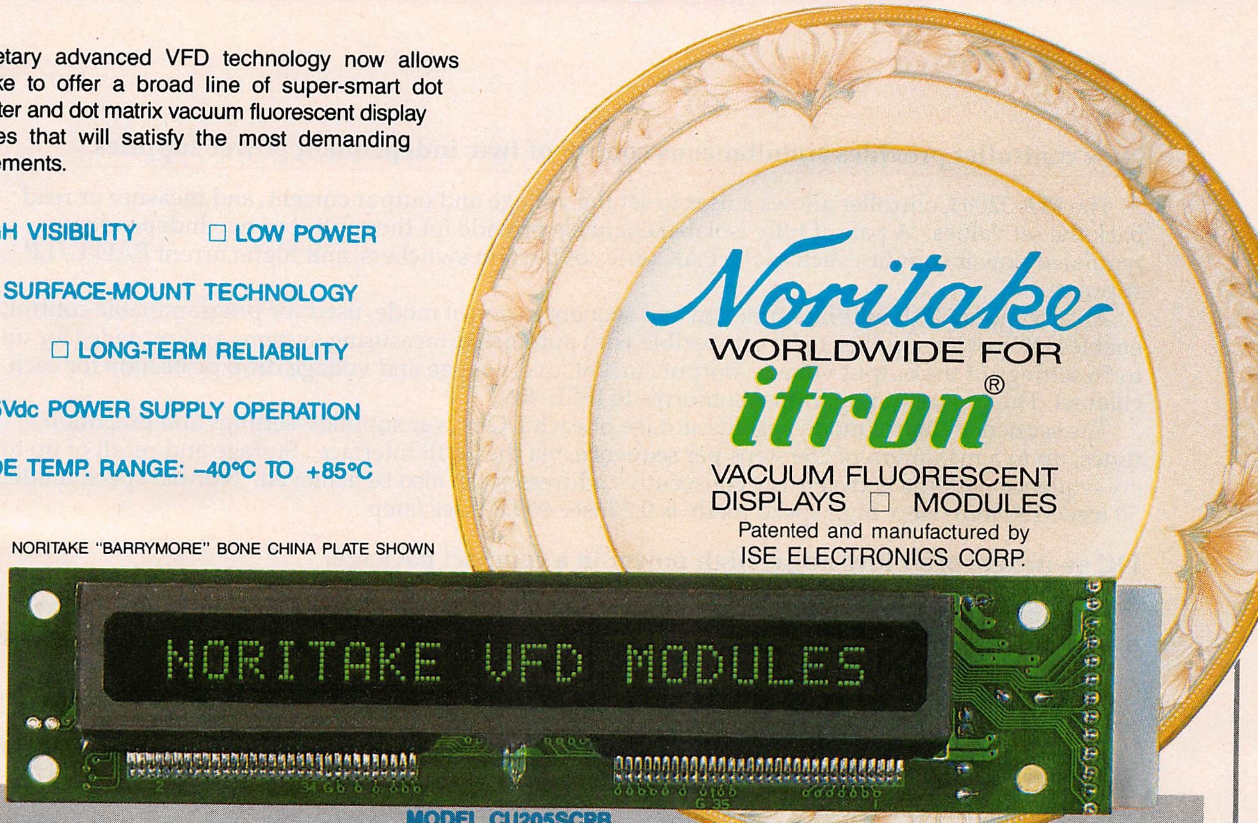

MODEL CU205SCPB

DOT CHARACTER DISPLAY MODULES

CHARACTER FORMAT	MODEL NUMBER	NUMBER OF CHARACTERS	CHARACTER HEIGHT (MM)	INPUT (SERIAL/ PARALLEL)	BI-DIRECT BUS	* WIDE TEMP. RANGE MODELS
5 × 7 DOT MATRIX	CU165SCPB-S	1 × 16	5.0	S/P		
	CU169SCPB-L	1 × 16	9.0	P	x	
	CU205SCPB-S	1 × 20	5.0	S/P		
	CU209SCPB-L	1 × 20	9.2	P	x	
	CU2015SCPB-L	1 × 20	15.1	P	x	
5 x 7 DOT MATRIX PLUS CURSOR	CU406SCPB-S	1 × 40	5.0	P	x	
	CU20026SCPB-S	2 × 20	5.1	P	x	x
	CU40026SCPB-S	2 × 40	5.0	P	x	x
	CU40046MCPB-S	4 × 40	5.0	S/P	x	x
	CU40066MCPB-S	6 × 40	5.0	S/P	x	x
	CU40086MCPB-S	8 × 40	5.0	P	x	x

*OPTIONAL

DOT MATRIX DISPLAY MODULES

DOT MATRIX FORMAT (DOTS/LINE × NO. OF LINES)	MODEL NUMBER	NO. OF LINES AND CHARACTERS/LINE (5x7 DOT CONFIGURATION)	GRAPHICS CAPABILITY
192 × 16 (3072 DOTS TOTAL)	GU192X16	2 × 32	YES
256 × 16 (4096 DOTS TOTAL)	GU256X16	2 × 42	YES
256 × 64 (16,384 DOTS TOTAL)	GU256X64	8 × 42	YES

The models shown are typical of the broad selection available on an immediate delivery basis. Contact our nearest sales office or representative for counsel on the best Noritake VFD for your application, as well as for details on costs, custom designs, deliveries, etc.

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Vol. I

Power Currents

Fall '90

New controller provides simultaneous control of two, independent power supplies.

The PIA 3200 Controller allows a user to set the voltage and output current, and measure or read back the set values. A pair of fully isolated channels provide for the control of two independent, regulated power supplies such as the PAK series of burn-in switchers, and high-current PAD-L/LP supplies.

An advanced GPIB interface function and sequence control mode, used for programmable control, enables DC power supplies to be compatible with automated measuring systems and provides for up to 56 settings of the output voltage, output current, overvoltage and voltage drop protection for each channel. The programming format conforms to IEEE-488.

The sequence control mode permits storage of each DC power supplies' settings and execution times, up to a maximum of 256 steps per sequence, via the GPIB interface. Storage and recall of up to six sequence patterns between any consecutive addresses can also be achieved. Normal speed mode is 50 msec-130 min/step; high speed mode is 0.2 msec-999.8 msec/step.

DC switchers offer low-noise, high power in a compact package.

New, low-noise DC CC/CV power supplies combine high current, small size and high power density for systems or bench applications. Output voltages range from 0-6 to 0-60 VDC with capacities of 350 W, 700 W and 1000 W.

Power densities of the PAK series range up to 2.5 watts per cubic inch. A typical 1000 W supply is packaged in a 19-lb. 5" x 8" x 14" enclosure.

Overall efficiency of 80% reduces power consumption, system heat radiation, and cost per watt. Line and load regulation averages ± 0.30% over the full input range. Ripple is typically 2% of nominal output at full load current.

New 50 W, 150 W and 300 W modular electronic loads can test multiple output power supplies, batteries, capacitors, and process control I/O ports.

These rack-mounted loads are ideally suited for use in systems applications such as burn-in power supply testing and battery and capacitor discharge tests.

A single rack mount, for example, accommodates up to eight 50-watt, four 150-watt, two 300-watt loads or various combinations up to 600 W. Depending upon the capacity, input voltages may range from less than 2 to 60 VDC.

The constant current, contact voltage and constant resistance modes may be remotely controlled using external voltage. Computer control for the PLZ-WU series is available using the GPIB bus.

New software-controlled power test systems provide fast, flexible test solutions without expensive programming.

The KITS (Kikusui Intergrated Test Systems) software package, built around National Instruments Lab Windows™, is a powerful window-oriented, menu-driven environment with interactive developmental capabilities that allows the user to plug in a variety of programmable instruments from various manufacturers. Directly available from Kikusui are digital scopes, electronic loads, AC & DC power sources and hi-pot test systems. The system provides optimal instrument control, ease of programming and simplified characterization of the Unit Under Test (UUT). In addition to running tests, this combination hardware/software system offers the necessary tools to analyze, display and store test parameters and data.

Kikusui International

19601 Mariner Avenue, Torrance, CA 90503
800/545-8784 or 213/371-4662

6801/6301/68HC11 8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: From less than $3 to $20 (1k).
SECOND SOURCE: Hitachi, SGS Thomson, and Toshiba. Hitachi second-sources the 6801 and calls the part 6301. SGS Thomson sources the 6801. Toshiba is a second source for 68HC11 devices.

Description: 6801 is a large, expandable, single-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8×8-bit multiplication, and a multifunction 16-bit timer. 68HC11 has a second 16-bit-wide register; an 8-function timer; a 2-function pulse accumulator; an enhanced UART (SCI); a 1-MHz serial shifter; an 8-channel, 8-bit A/D converter; and a 512-byte EEPROM. One-time-programmable/mask versions include as much as 24k-bit on-chip EPROM/ROM and built-in device selects and bank switching circuits for as much as 20-bit addressing.

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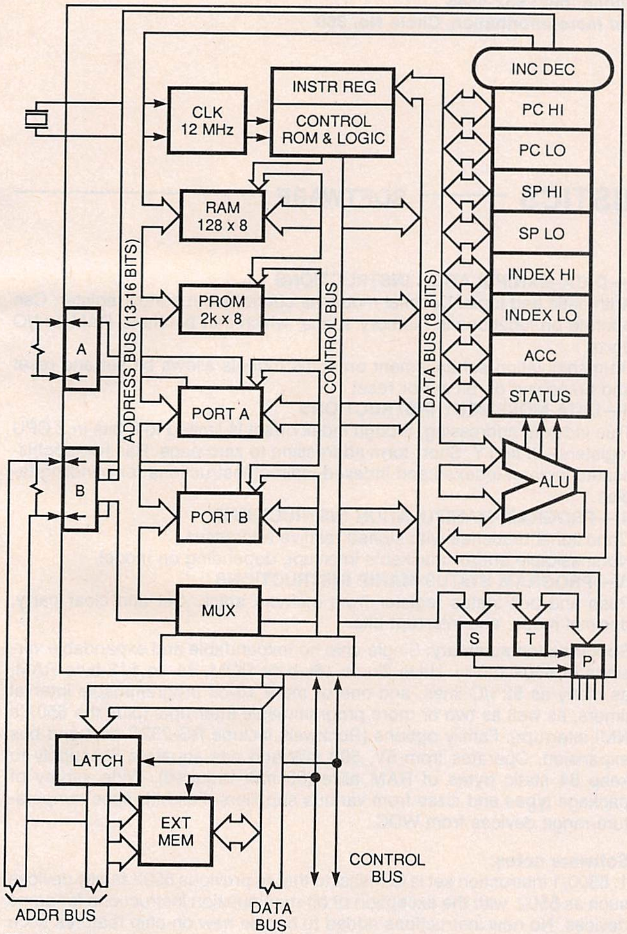
Status: This family has been well received. Motorola is now following migration of customers to more powerful single-chip devices and is concentrating on the 68HC11 enhancement of the 6801, such as increased on-chip EEPROM. The company is also adding various peripheral functions in many of the family derivatives.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for 6801. See table for other family members.
2. Motorola provides one-time-programmable versions of some HC11 family members that have EPROM program memories in inexpensive windowless packages for one-time programming in moderate-volume production (to 10k).
3. Motorola's 68HC11 is a much enhanced 6801. 68HC11A8 has a 512-byte EEPROM; 68HC811E2 has a 2k-byte EEPROM; 68HC711E9 has a 12k-bit EPROM; 68HC711K4 has a 24k-bit EPROM.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of 2 accumulators, including 8×8-bit multiply. 68HC11 has additional 16-bit operations, integer and fractional divides, and bit manipulation.
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
Can list-process efficiently with the index register (2 on 68HC11) and can add accumulator to index register within a 64k-byte range.
Relative addressing allows data relocation.
Has 16-bit load and store.
III—PROGRAM-MANIPULATION INSTRUCTIONS
Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM.
Eight levels of prioritized, vectored interrupts (21 on 68HC11).
IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Instructions for storing status register or transferring to or from accumulator. 68HC11 has additional active bits related to stop mode.
V—POWER-SAVING INSTRUCTIONS
6301 has sleep instruction. 68HC11 has Stop and Wait instructions similar to 146805 but with disabling provision via a bit in the status register.

Specification summary: Expandable single-chip μC with common-memory architecture in which all instructions, data, I/O, control, and data registers share the same memory space. This scheme allows I/O to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and 88 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in the table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 4 MHz for 68HC11. The 6801 is fabricated in NMOS, the 6301 is fabricated in CMOS, and the Motorola 68HC11 is fabricated in static CMOS to allow dormant, micropower "asleep" state. 6801 in 40-pin DIP, 6301 in 64-pin DIP and flatpack, and 68HC11 in 48-pin DIP and 52-, 68-, and 84-pin PLCCs.

Software notes:
1. 6801 has all 6800 μP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set with 88 additional op codes.

Part	Description	Memory			Internal bus speed	I/O		Timer event ctr	Pins
		On chip							
		ROM	RAM	Ext		Parallel	Serial		
6801	Expandable 1-chip μC	2k	128	64k	0.5M–2.0M	29	3	3×16	40
68701	EPROM version of 6801	2k	128	64k	0.5M–2.0M	29	3	3×16	40
6803	ROMless 6801	—	128	64k	0.5M–2.0M	13	3	3×16	40
68HC11	CMOS with UART, serial I/O, 8-bit A/D converter	24k (Also 512 EEPROM)	768	2M	0–4M	28 32	6	4×16	48 (DIP) 52, 68, 84 (QUAD)

Note: Parts have two external interrupts.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: For 6801 family, M68701EVM is an evaluation module that has a port for terminal and a port for any RS-232C host and will program 68701 EPROM parts. For 68HC11, the similar M68HC11EVM. Also M68HC11EVB boards ($168.11) for evaluating single-chip configuration of HC11s. For both 6801 and 68HC11, the under $3000 PC-based CDS8 Jewelbox series of development systems features real-time, noninvasive in-circuit emulation with real-time tracing and other debugging capabilities.
From SGS Thomson: INICE4-8 development and emulation system.
From others: Third-party hardware development systems, such as CT68HC11 ($5000 to $6000) from Ashling Microsystems Ltd (Limerick, Ireland).

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733. C compiler runs on Unix System V for 68HC11. For the least expensive approach, use 6801 parts with Lilbug monitor in on-chip ROM (MC6801L1).
From SGS Thomson: Interactive development software.
From others: Cross macroassemblers and linking loaders, some relocatable, run on popular minis and personal computers. For example, C compiler from Archimedes (San Francisco, CA) runs on the IBM PC ($995) and DEC VAX ($3995 to $5995).

6500/1, 65C124, 65C265, 50740, 37700 8-BIT (AND 16-BIT) NMOS AND CMOS

AVAILABILITY: Now for all NMOS and most 8-bit CMOS parts.

COST: Prices range from $2 to $20 according to complexity of part and volume. Volume leader Mitsubishi's prices range from $4 to $60.

SECOND SOURCE: NCR (licensed) and California Micro Devices for Rockwell NMOS parts. Western Design Center (WDC) has licensed a number of suppliers worldwide for its CMOS designs.

CORE: Standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, and several others. Widely used because of compact 6502 die size.

Description: There are three different sources for single-chip versions of the 6502 µP: the original 6500/1 NMOS family from Rockwell, the new 65C124 and -134 CMOS family from WDC, and the 50740 CMOS family from Mitsubishi. Most parts are 100% software compatible with 6502, although in some cases enhanced instructions such as bit manipulation have been added. Because of the small size of the 6502 core, many parts take a standard-cell ASIC approach. Vendors claim these 1-chip sets have a speed advantage over competing single-chip devices due to the 6502's 2-cycle bus and pipelining.

Status: Mitsubishi's 50740 Series is a top volume leader among 8-bit µCs. Mitsubishi's explanation for the part's success is its use in Japanese consumer products. Standard or custom 50740s are found in products from Hitachi, JVC, Sanyo, and Minolta.

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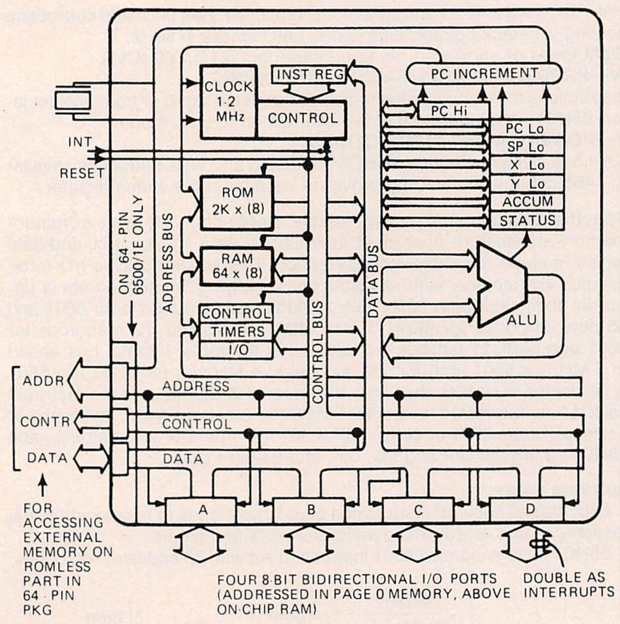
Mesa, AZ 85203
Phone (602) 962-4545
For more information, Circle No. 360

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:

1. Diagram favors initial Rockwell 6500/1 version. Most other versions are more complex.
2. Mitsubishi 740 Series parts are all CMOS and have as many as 16k bytes of ROM and 512 bytes of RAM. Some models have special functions such as UARTs, 8-bit A/D converters, LCD drivers, or high-voltage (−35V) outputs. Some have 56 pins of I/O.
3. Mitsubishi's new CMOS M37700 version has an 8-bit external/16-bit internal data bus, much like the 68C816 version of the 6502 µP. On chip, it can have as many as 32k bytes of ROM, 2k bytes of RAM, eight 16-bit timers, 2 UARTs, 1 watchdog timer, and an 8-channel 8-bit ADC. Memory is expandable to 16M bytes off chip.
4. WDC's first part, 65C124, has been joined by 65C134—a 6502 core µP—which includes a low-power LAN connection and UART.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports.
Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset.

II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset is limited to 8 bits in 2 CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables.

III—PROGRAM-MANIPULATION INSTRUCTIONS
Conditional branches with signed relative addresses.
Nonmaskable and/or maskable interrupt, depending on model.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits.

Specification summary: Single-chip nonexpandable and expandable versions of 650X family. Have 2k- to 16k-byte ROM, 64- to 512-byte RAM, as many as 52 I/O lines, and one or more 16-bit programmable interval timers, as well as two or more programmable interrupts (plus the 650X's NMI interrupt). Family options (Rockwell) include RS-232C port and bus expansion. Operates from 5V, 500 mW and has separate 5V supply to keep 64 static bytes of RAM alive (50 mW required). Wide variety of package types and sizes from various suppliers. Full MIL-spec temperature-range devices from WDC.

Software notes:

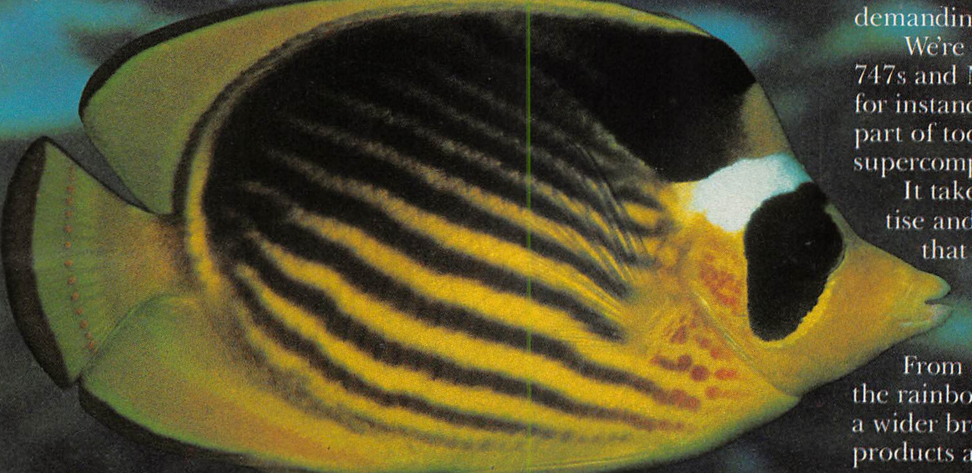
1. 6500/1 instruction set is identical to that of previous 650X family devices such as 6502, with the exception of bit-manipulation instructions for some devices. No new instructions added to handle new on-chip features such as timers and I/O because the µP handles them as if in external memory space.
2. Mitsubishi chips have some added instructions.
3. WDC's 65C134 adds some instructions and an operating voltage range of 1.8 to 5.25V.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: R6500/1 personality card ($995), which plugs into LCE System ($1250) uses emulator part, the 64-pin 6500/1E ($75). Backpack part will be ROMless 40-pin R6500/1EAB ($42), into which you can plug industry-standard EPROMs.
From Mitsubishi: Debugging machine PC4000E ($1000) with in-circuit-emulator (ICE) cards for each device model ($750 to $1500).
From WDC: Toolbox Design System ICE for W65C124 runs on an Apple IIGS host and can communicate with an IBM PC via a serial port ($4995).

From Rockwell: Because the 6500/1 emulator runs on LCE system and Aim-65 (Dynatem, Irvine, CA), you can use existing 6502 program-development software. A debugging monitor is available for all 6500/1 and 6500/11 devices, and the macroassembler supports enhancement instructions. Cross software available.
From Mitsubishi: Cross software for MS-DOS. (Has plans for a C compiler and Forth interpreter.)
From WDC: Many software packages available from third parties for the W65C02/W65C816 µPs.

Thanks to us the government knows this is not an enemy sub.



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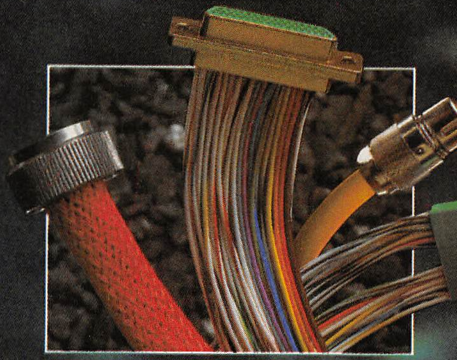

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CIRCLE NO. 83

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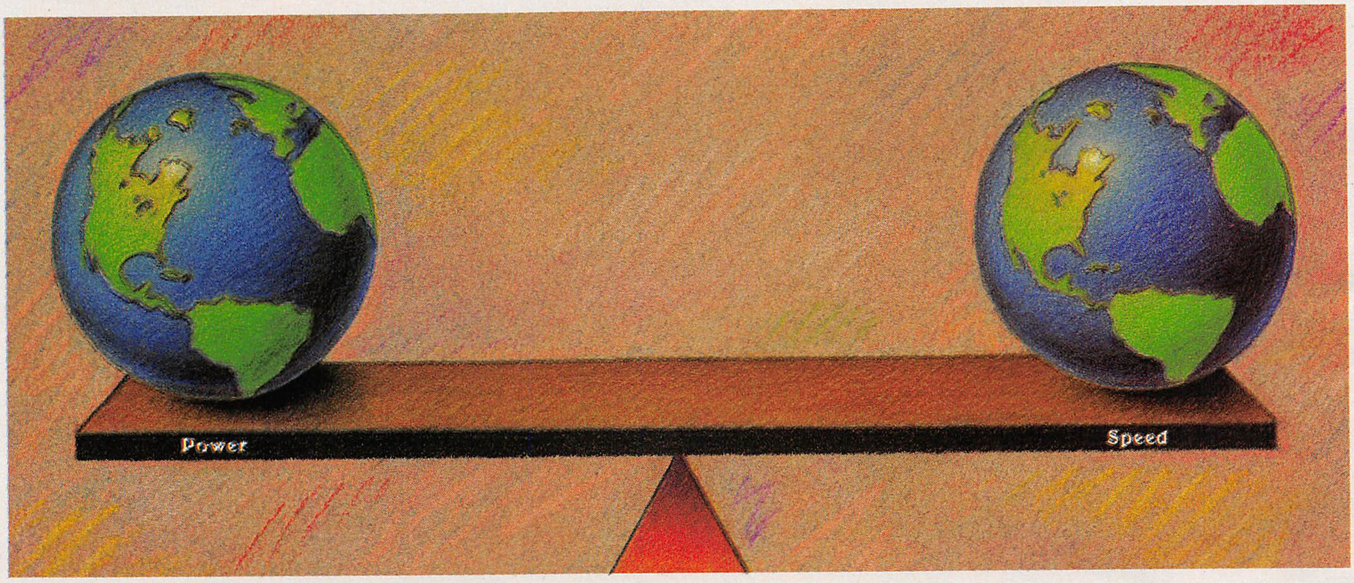

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CIRCLE NO. 14

Z8, SUPER8

8-BIT NMOS AND CMOS

AVAILABILITY: Now for ROMless and 1k-, 2k-, 4k-, and 8k-byte parts; 2k- and 8k-byte EEPROM; and one-time programmables at 8, 12, 16, and 20 MHz. Sharp and Zilog have CMOS now. SGS Thomson has 4k-byte EPROM and 8k-byte ROM.

COST: Less than $3.50 for NMOS Z8 in volume. $3.60 for NMOS Super8 in volume. (28-pin version for $1.) Less than $5 for CMOS Z8.

SECOND SOURCE: SGS Thomson (licensed); Sharp for both NMOS and CMOS; VLSI Technology for CMOS.

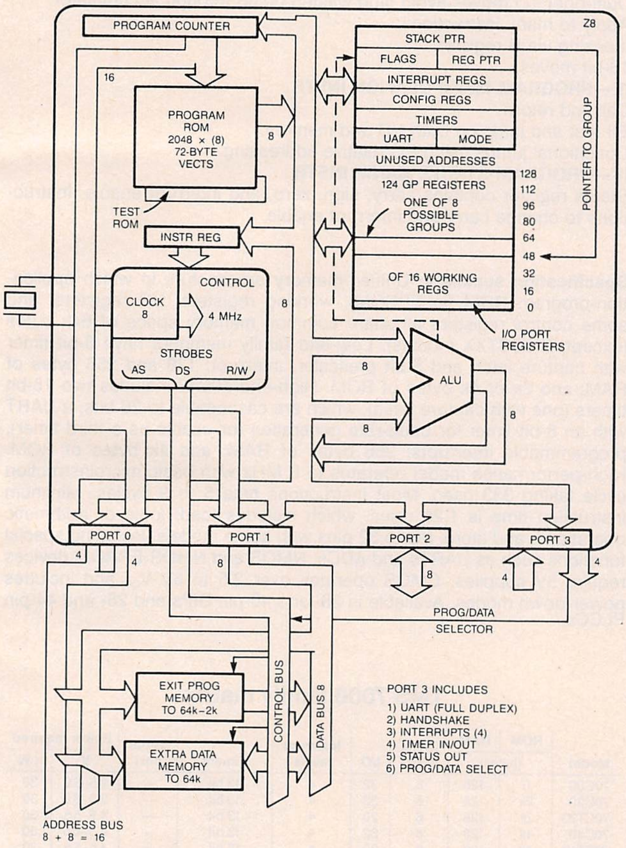
CORE: From Zilog and VLSI Technology. SGS Thomson aims to convert NMOS Z8 designs to its CMOS ST9 core.

Description: Z8 is a single-chip μC that is a composite of many machines. You can't necessarily use its powerful features simultaneously, a common problem with single-chip units. Not really compatible with supplier's Z80 or Z8000 because architecture is so different; closest to Z8000. However, slave Z8 versions interface to Z80 and Z8000 buses. Super8 version has more of everything: more data and program memory, more on-chip peripherals, more instructions.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000
For more information, Circle No. 361

Status: According to Zilog, Z8 volume is growing at a compound annual growth rate of 33% and Z8 has had several hundred design wins (many in Far East); some of these design wins are now going into production. Meanwhile, second-source SGS Thomson has turned its CMOS efforts to its ST9, a proprietary enhancement of the Z8, which SGS Thomson uses for an ASIC building block.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:

1. Diagram applies to basic 2k-byte version. Many other versions exist.
2. The 124 working registers (272 on Super8) are truly general purpose. Any one can be used as an accumulator or indexer.
3. The register pointer singles out a "workspace" of 16 working registers for fast access. Eight such workspaces are possible in the 124-register space (16 in Super8) and provide a mechanism for fast context switching upon interrupt.
4. SGS has not announced any CMOS Z8s. Instead it has introduced an S9 ASIC core in 1.5-μm CMOS. According to SGS, this core reaches 12 MHz (24-MHz external clock).

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, and subtract with borrow.
Multiply and divide added to Super8 version.
Logicals: AND, compare, complement, OR, and exclusive OR.
Rotates and swaps.
Bit manipulation: test under mask, test complement under mask, and logical tests of bits.

II—DATA-MOVEMENT INSTRUCTIONS
Address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative.
Block transfer: load constant autoincrement, load external autoincrement.
Load: clear, load, load constant, load external, and pop and push.

III—PROGRAM-MANIPULATION INSTRUCTIONS
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, jump relative conditional, and return.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Set, reset, and complement of carry flag.

Note: Ability to set, reset, and test any bit or combinations of as many as 8 bits lets any byte function as a user flag register.

Specification summary: Unique architecture with 3 memory spaces: program memory (0, 2k, 4k, or 8k bytes in internal masked ROM; rest to 64k bytes can be external), data memory (to 64k bytes external), and CPU register file (256-byte space that includes 124 general-purpose working register/accumulators). Executes 129 instructions at 0.6 to 3.0 μsec at 8-MHz internal clock (16-MHz oscillator). Has built-in duplex UART (96k bps) and two 8-bit timers, each with 6-bit prescaler. Enhanced Super8 has 352 bytes of on-chip data and control registers, 256 of which are general purpose. New multiply and divide instructions on Super8. Its on-chip peripheral functions include DMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has 600-nsec interrupt response with 37 interrupt sources.

Software note:
The data- and program-manipulation instructions use the working registers in the CPU. The instructions that apply to the external data RAM are essentially just loads and stores. (There is a similarity to RISC philosophy.)

HARDWARE — SUPPORT — SOFTWARE

Development packages are available from JK Engineering (Singapore, 65-744-8414). In the US, IAM (Sacramento, CA) distributes JK Engineering's products. Development packages in various configurations are also available from Zilog Inc (Campbell, CA) and Inner Access (Belmont, CA). Emulation packages are available from Orion Instruments (Redwood City, CA), Microtek (Beaverton, OR), Creative Technology (Atlanta, GA), and Sophia Systems (Santa Clara, CA). This list isn't exhaustive.

Software development tools are available from Allen Ashley (Pasadena, CA), Avocet (Rockport, ME), Relational Memory Systems (San Jose, CA), and Western Wares (Norwood, CO). You can purchase compiler software from Micro Computer Compilers (Hopewell, NJ), 2500 AD (Buena Vista, CA), and Inner Access (Belmont, CA). This list isn't exhaustive.

7000 FAMILY

8-BIT CMOS

AVAILABILITY: Now.

COST: TI pricing: $1.60 to $3.50 (100k) for standard CMOS masked-ROM versions.

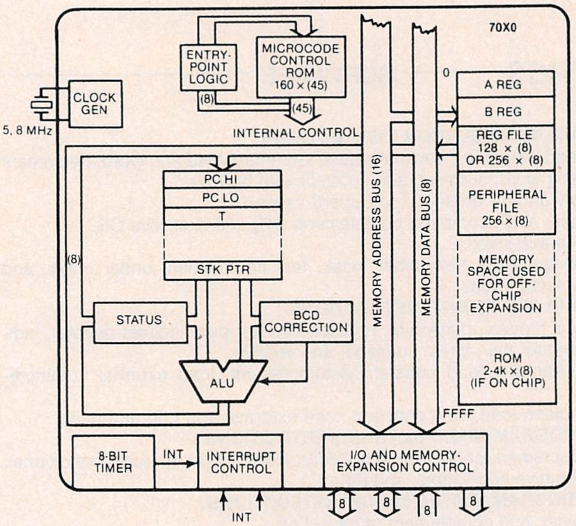
SECOND SOURCE: Microchip Technology and Seeq for NMOS versions only. Note that each supplier is extending the family in different directions, so direct second sourcing is limited.

Description: Software-compatible family of NMOS and CMOS 8-bit, expandable single-chip μCs. A full-duplex UART, enhanced timers, and interrupts are incorporated in high-end family members. Instructions typically perform combined load, operation, and store functions, thereby increasing overall system performance and code efficiency.

Texas Instruments Inc
Microprocessor and Microcontroller Products Div
Box 809066
Dallas, TX 75380
Phone (800) 232-3200
For more information, Circle No. 362

Status: Primary supplier TI has switched its emphasis to CMOS models with expanded features. Low-end devices (70CT20/40) offer an alternative for designers who are using 4-bit μPs but seek a low-cost 8-bit alternative.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware note:
Supplier uses a "strip-chip" architecture to keep registers and control elements in isolated, self-contained modules in silicon, then uses a single layer of metal to interconnect chip. This approach is similar to the cell-library, semicustom approach and useful for the same reason. Changes can be made easily, which helps TI bring out new models or give large customers special variants.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8×8-bit multiply, and BCD.
Logicals, increment, and decrement.
Rotates right and left. Bit test.

II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Apply to many instructions.
Indexing via B register.
16-bit moves.

III—PROGRAM-MANIPULATION INSTR
Call and return.
Bit test and jump on both I/O and memory.
Conditional jumps using PC-relative addressing.

IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, and interrupt enable. Instructions to change carry and interrupt enable.

Specification summary: Unified-memory architecture in which application-program ROM (in EPROM), working registers, I/O registers, and some control registers all share common memory space of 64k bytes (except TI 70CTXX models). Low-end family members have 8-bit timer with capture latch and 5-bit prescaler; interrupt; 128 and 256 bytes of RAM; and 2k or 4k bytes of ROM. High-end 70C42 includes two 16-bit timers (one with capture latch), which are cascadable to 26 bits; a UART with an 8-bit timer for baud-rate generation (or usable as a third timer); programmable interrupts; 256 bytes of RAM; and 4k bytes of ROM. High-performance model operates to 6 MHz with basic microinstruction cycle taking 333 nsec. Most instructions take 5 to 9 cycles. Minimum instruction time is 1.25 μsec, which includes load, logic or arithmetic operations, and store. I/O to 32 pins with some models, including special functions such as UARTs and ADCs. NMOS and NMOS-EPROM devices require 5V supplies; CMOS operates over 2.5 to 6V V_{CC} and includes power-down modes. Available in 28- and 40-pin DIPs and 28- and 44-pin PLCCs.

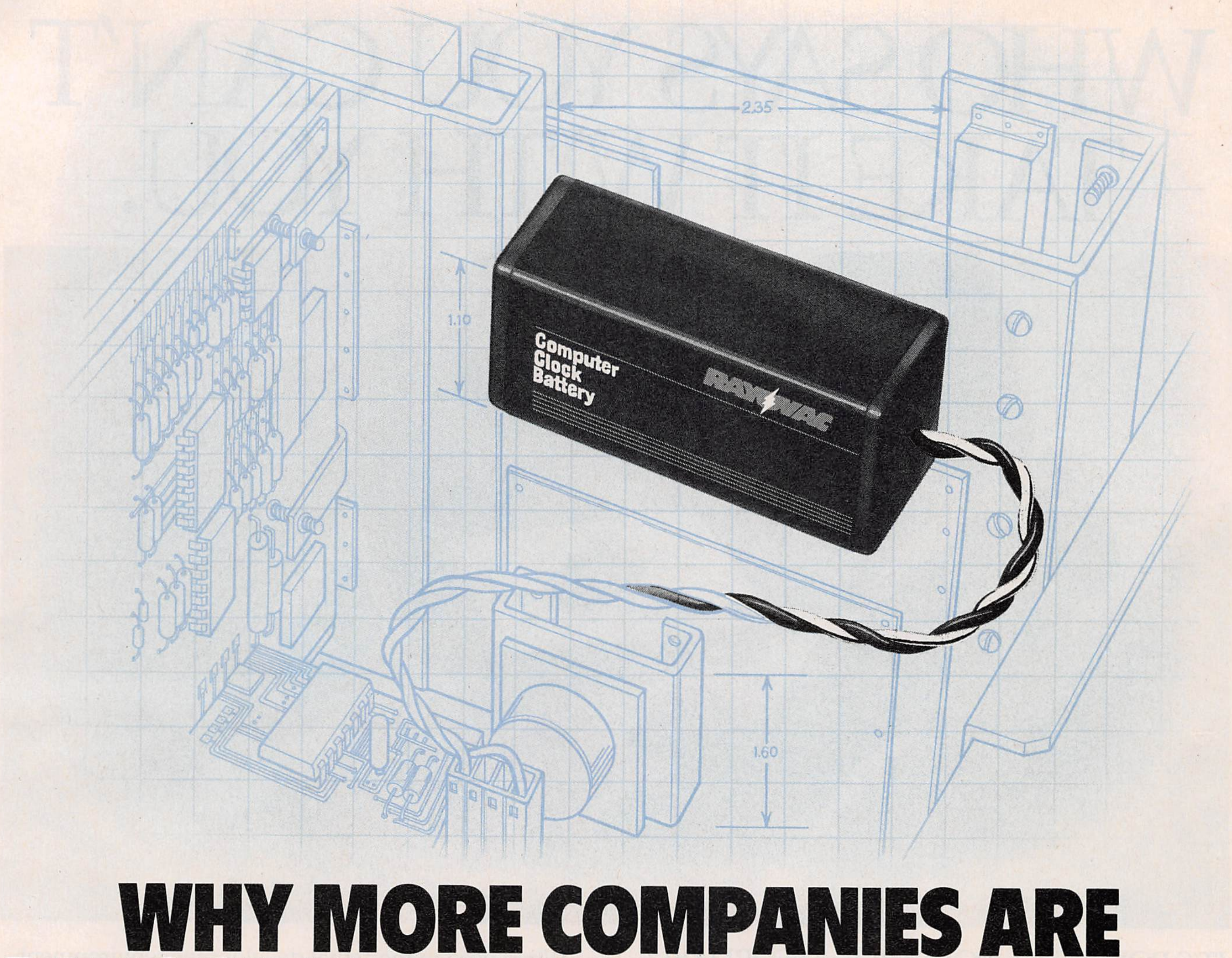
TMS 7000 family matrix

Model	ROM	RAM	Clock (MHz)	I/O	Interrupt levels	Timers	Serial port	Power required V	Power required mW
	(bytes)								
70C00	0	128	6	32	4	13 bit	—	2.5–6.0	30
70C20	2k	128	6	32	4	13 bit	—	2.5–6.0	30
70CT20	2k	128	6	20	4	13 bit	—	4.5–5.5	30
70C40	4k	128	6	32	4	13 bit	—	2.5–6.0	30
70CT40	4k	128	6	20	4	13 bit	—	4.5–5.5	30
70C02	0	256	6	32	6	21, 21, 10 bit	UART	2.5–6.0	30
70C42	4k	256	6	32	6	21, 21, 10 bit	UART	2.5–6.0	30

HARDWARE — SUPPORT — SOFTWARE

From TI: XDS development system ($5900). It provides in-circuit emulation, target-system debug (with breakpoints and logic-state trace), and RS-232C link to host computer or terminal. EVM evaluation board ($795) provides in-circuit emulation, programs SE77C42 and EPROMs, and has serial interface to standard terminals. Piggyback devices accept 27C64 and 27C128 EPROMs. SE70CP160 CMOS piggyback device supports prototyping for 70C20, 70CT20, 70CT40, and 70C40 μCs. SE70CP162 CMOS piggybacking device and SE77C42 support prototyping for 70C42.

From TI: Cross-assembler and linker to run on MS-DOS-based PC that may serve as host for XDS. DEC VAX VMS assembler/linker support is also available.
From Cybernetic Micro Systems (San Gregoria, CA): Assembler, simulator, and debugger to run on IBM PC.
From Allen Ashley (Pasadena, CA): Cross-assemblers and emulators to run on IBM PC.
Literature: TI 7000 family data manual with applications.



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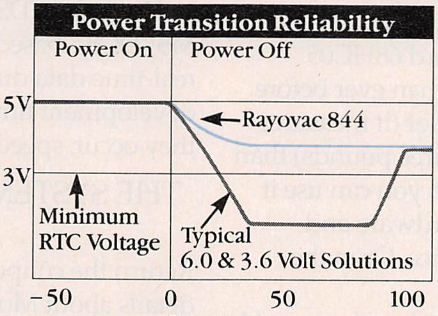

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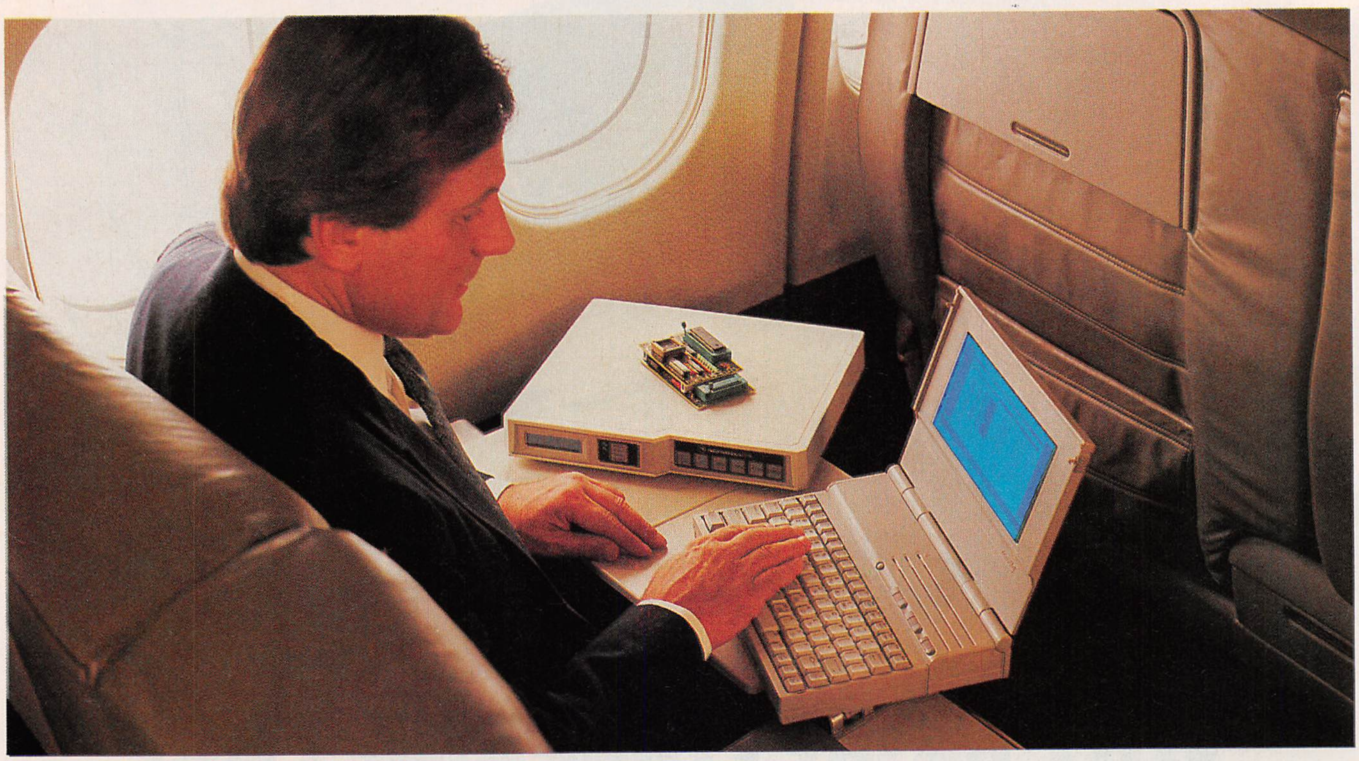
CIRCLE NO. 115

WHO SAYS YOU CAN'T TAKE IT WITH YOU.



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How? Simple. The CDS8/05 is smaller (it measures just 12" x 11" x 2" and weighs under three pounds) than any other system in its power range. So you can use it with a portable laptop PC to debug hardware and software *anywhere*: At home. In the office. Or in the field.

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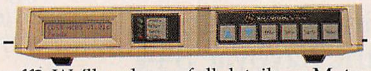

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8085AH/80C85

8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: Prices for these older multisourced parts have dropped to $1 and below, with prices as low as $0.65 for volume purchases. CMOS parts, especially faster ones, are more expensive. Radiation-hardened CMOS parts are very expensive ($300 to $800).
SECOND SOURCE: 8085: NEC, Toshiba, and Mitsubishi. 80C85: Harris, Newbridge Microsystems, and Oki. Harris supplies nuclear-radiation-hardened CMOS to military and aerospace customers.
CORE: Newbridge offers 80C85B macrocells in its ASIC library.

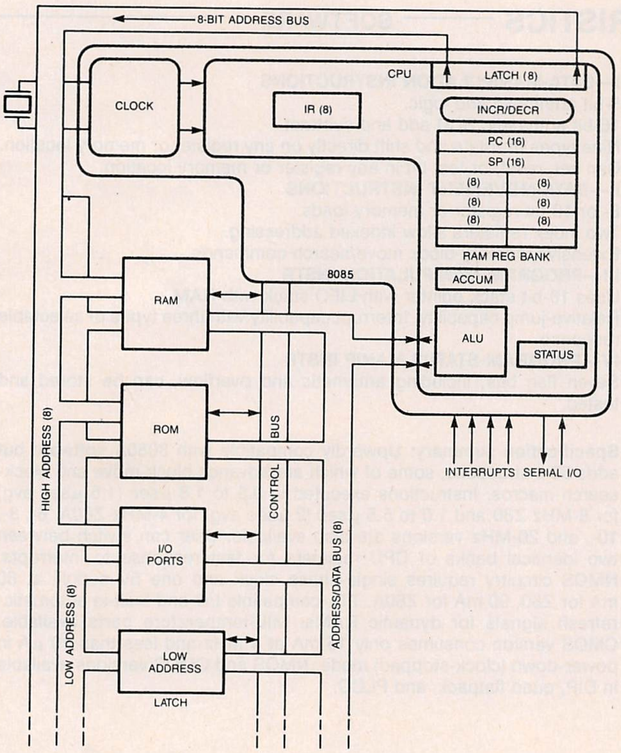
Description: Based on the older 8080 μP, this family has proven to be a good general-purpose, midrange μP, though not the most efficient one for small programs. 8085 executes 8080 instructions, but with simpler hardware. Z80 (see pg 120) is an enhanced 8080 but has different package pinouts and bus operation. The new 8086 (see pg 128) is only vaguely software compatible, but the 8-bit-bus 8088 version of 8086 can interface to 8080 and 8085 peripherals.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 363

Status: The venerable 8080—the μP that gave legitimacy to the μP revolution—is obsolete. Sales of the 8085 are also falling off, according to Dataquest figures.

CHARACTERISTICS

HARDWARE



Hardware note:
The 8085 differs from the 8080 in that the 8085 has an on-chip clock, needs only a 5V supply, and has relaxed memory-access time. But because it multiplexes the lower 8 bits of address on data bus, it's not pin compatible with 8080. New pins gained by multiplexing implement address-latch strobe, four additional interrupts, and two serial-I/O lines. For small "few-chip" μP systems, a designer can use 8155/56 and 8355/8755 combo chips with built-in address latches.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
BCD arithmetic.
Double-precision operations (instructions string 2 data bytes together as 16-bit word).
II—DATA-MOVEMENT INSTRUCTIONS
Uses 3 pairs of so-called general-purpose registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can perform multiple indexing with these, but takes additional steps compared with classical index-register concept. 8085 has two additional instructions—RIM and SIM—that interface with new serial-I/O pins and interrupt system.
III—PROGRAM-MANIPULATION INSTR
Uses stack pointer to create LIFO stacks in external RAM for unlimited subroutine nesting.
All GP registers can be incremented and decremented.
Multiple-interrupt capability.
Bus controls allow addition of DMA.
IV—PROGRAM-STATUS-MANIP INSTR
Software access to status register.

Specification summary: Common instruction and data architecture (64k bytes) with optionally separate I/O space (256 addresses). Three 16-bit pointer registers allow efficient addressing of 64k-byte main-memory space. 78 basic instructions with 2-μsec (typ) register-to-accumulator addition-execute time. 8085A has on-chip clock and needs only 5V. 5-MHz and CMOS versions of the 8085A available. The Newbridge Microsystems (Calmos) version officially supports the extended 8085 instruction set.

SUPPORT

HARDWARE

Most of the vendors of third-party μP development systems have included 8080/8085 development components as a routine part of their catalogs. Typically, these systems use IBM PCs as hosts.

SOFTWARE

Most of the many companies that supply 8080/8085 development systems also supply the software. Also, many software houses have 8080/8085 software in every conceivable category.

Z80

8-BIT NMOS AND CMOS

AVAILABILITY: Now for 6-, 8-, 10-, and 20-MHz NMOS and CMOS versions.

COST: Because of the many aggressive second sources for this most widely used part, NMOS prices have dropped to between $0.80 and $1.10; CMOS prices have dropped to between $1 and $1.20 in high volume. The 10-MHz CMOS part costs $2.50 (100).

SECOND SOURCE: Goldstar, NEC, SGS Thomson, Sharp, and Toshiba. Goldstar, SGS Thomson, Sharp, and Toshiba, as well as Zilog, have CMOS versions. Additional sources mentioned by Zilog are VLSI Technology and Rohm.

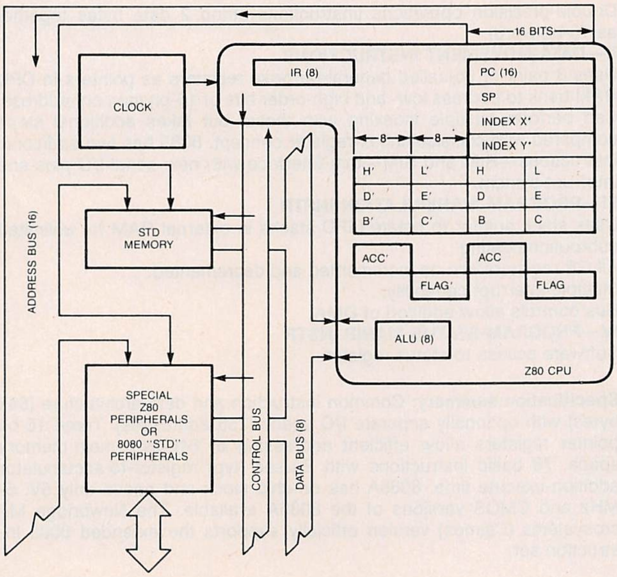
CORE: Zilog and Hitachi use the Z80 µP as an ASIC core in their enhanced versions of this core, the 64180 and Z280. Zilog, Hitachi, and Toshiba are building a range of specialized processors around the Z80 core.

Description: Superset of widely used 8080/85; adds hardware and software features. Not pin-for-pin compatible with 8080 or 8085 but can use 8080 software and peripherals—although to do so would not take full advantage of Z80 and its peripherals, and it might require additional logic for interfacing. The Z80 and its peripherals are now available in quad flatpacks and all peripherals have been upgraded to run at 10 MHz. The 20-MHz version is only available from Zilog.

Zilog Inc
Intelligent Peripheral Controllers Product Line
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000
For more information, Circle No. 364

Status: By far the most successful 8-bit µP. The Z80 is still being used in new designs but may be superseded by the new enhanced versions. Of these, the Zilog Z180/Hitachi 64180 seems to be the most popular, but the Zilog Z280 represents the greatest Z80 enhancement. The Z80's momentum will probably last for the rest of this century, especially in ASIC-core form.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8-bit arithmetic and logic.
16-bit arithmetic BCD add and subtract.
Nine types of rotate and shift directly on any register or memory location.
Can set, reset, or test bit in any register or memory location.

II—DATA-MOVEMENT INSTRUCTIONS
8- or 16-bit register or memory loads.
Two index registers allow indexed addressing.
Extensive memory-block move/search commands.

III—PROGRAM-MANIPULATION INSTR
Uses 16-bit stack pointer with LIFO stack with RAM.
Relative-jump capability. Interrupt capability with three types of selectable response.

IV—PROGRAM-STATUS-MANIP INSTR
Seven flag bits, including arithmetic and overflow, can be stored and tested.

Specification summary: Upwardly compatible with 8080A software but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 0.5 to 1.8 µsec (1.5 µsec avg) for 8-MHz Z80 and 1.0 to 5.5 µsec (2 µsec avg) for 4-MHz Z80A. 6-, 8-, 10-, and 20-MHz versions are also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires single-phase clock and one 5V supply at 60 mA for Z80, 90 mA for Z80A. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. MIL-temperature parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 µA in power-down (clock-stopped) mode. NMOS and CMOS versions available in DIP, quad flatpack, and PLCC.

Hardware notes:

1. Support chips include peripheral interface, timer, serial communications, and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. All Z80 enhancements are in CMOS. The first is the Zilog Z180/Hitachi 64180, to which many Z80 designers are converting. The second is the supplier's Z280, which boosts the Z80 into minicomputer performance. In addition, the NEC 78XX single-chip device is similar. Most are covered elsewhere in this directory.

HARDWARE — SUPPORT — SOFTWARE

Some of the many third parties that supply Z80 hardware support are Applied Micro, Boston Systems, Emulogic, Hewlett-Packard, Huntsville Microsystems, Nicolet, Orion, Sophia Systems, Tektronix, Zax, and Z-World. Contact nearest Zilog sales office for more information.

A variety of software supports the Z80 including assemblers and cross-assemblers, software simulators, high-level-language compilers, the venerable CP/M operating system (Digital Research), and the MS/X operating system, which is popular in Japan. Other third-party suppliers include 2500 AD, Archimedes, Avocet Systems, Enertec, Huntsville Micro, Softaid, Software Development Systems, Microtec Research, and Z-World.

The MOST 80C51 Microcontroller Derivatives in the World

Philips Components-Signetics

80CXXX = ROM-Less   83CXXX = Masked ROM   87CXXX = EPROM/OTP

DEVICE	OTP & EPROM	ROM (bytes)	RAM (bytes)	8-BIT PORTS	SERIAL I/O		TIMERS	SPECIAL FEATURES	PACKAGES
					UART	I^{2}C			
8XC751 (1)	X	2K	64	2 + 3/8		X	1	24 Pin Skinny DIP	A28, F24, N24
8XC752 (1)	X	2K	64	2 + 5/8		X	1	8-bit A/D, PWM	A28, F28, N28
80C31/8XC51 (2)	X	4K	128	4	X		2	Industry Standard	A44, B44, F40, K44, N40
8XCL410	(3)	4K	128	4		X	2	Low Volt/Power (1.5 volts)	N40, T40
8XC851		4K	128	4	X		2	256 EEPROM	A44, B44, N40
8XC550	X	4K	128	4	X		3	8-bit A/D, WD	A44, B44, F40, K44, N40
8XC451	X	4K	128	7	X		2	7 I/O Ports	A68, F64, K68, N64
8XC852		6K	256	2/8			2	Smart Card, 2K EEPROM, CCU	Die only
8XC652	X	8K	256	4	X	X	2	8K ROM, I^{2}C Serial Bus	A44, B44, F40, K44, N40
80C32/8XC52 (2)	X	8K	256	4	X		3	Industry Standard	A44, B44, F40, K44, N40
8XC562	(4)	8K	256	6	X		4	8-bit A/D, PWM, WD, T2	A68, B80
8XC552	X	8K	256	6	X	X	4	10-bit A/D, PWM, WD, T2	A68, B80, K68
8XC053	(5)	8K	192	3 + 4/8			2	TV Display (OSD), PWM, D/A	N42
8XC054 (1)	X	16K	192	3 + 4/8			2	TV Display (OSD), PWM, D/A	N42
8XC654	X	16K	256	4	X	X	2	16K ROM, I^{2}C Serial Bus	A44, B44, F40, K44, N40
8XC592	X	16K	256	6	X		4	CAN Bus, 10-bit A/D, WD	A68, K68, B80
8XC528	X	32K	512	4	X	X	4	32K ROM, 512 RAM, WD	A44, B44, F40, K44, N40

Footnotes

(1) No ROM-less derivative available
(2) 80C31, 80C32 = ROM-less
80C51, 80C52 = Masked ROM
87C51, 87C52 = EPROM/OTP
(3) Piggyback available for EPROM development
(4) Use 87C552 EPROM/OTP
(5) Use 87C054 EPROM/OTP

Abbreviations

A/D = Analog-to-Digital Converter
PWM = Pulse Width Modulation
WD = Watchdog Timer to reset the microcontroller
T2 = Capture/Compare Counter/Timer with High Speed Outputs
I^{2}C = Inter-Integrated Circuit Serial Communications Bus
OSD = On Screen Display
D/A = Digital-to-Analog Converter
CAN = Controller Area Network Serial Communications Bus
CCU = Cryptographic Calculation Unit

Package Types

A = Plastic Leaded Chip Carrier (PLCC)
B = Plastic Quad Flat Pack (PQFP)
N = Plastic Dual In-line Package (PDIP)
F = Windowed Ceramic Dual In-line Package (CDIP)
K = Windowed Ceramic Leaded Chip Carrier (CLCC)
T = Plastic Very Small Outline Package (VSO)

98-8080-550

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80C51 MICROCONTROLLER DEVELOPMENT SYSTEM SUPPORT

COMPANY	ADDRESS	SUPPORT FUNCTIONS
ARCHIMEDES SOFTWARE	2159 Union Street San Francisco, CA 94123 (415) 567-4010	C - COMPILER FOR 8051 FAMILY
FRANKLIN SOFTWARE	888 Saratoga Ave. #2 San Jose, CA 95129 (408) 296-8051	C - COMPILER FOR 8051 FAMILY
METALINK	325 E. Elliot Road, Suite 23 Chandler, AZ 85225 (602) 926-0797	MICROICE + EMULATOR SUPPORTS 80C51 MICROCONTROLLER FAMILY
NOHAU	51 E. Campbell Ave. Campbell, CA 95008 (408) 866-1820	EMUL51-PC SUPPORTS 80C51 MICROCONTROLLER FAMILY

PROGRAMMING SUPPORT CONTACTS

BP Microsystems
10681 Haddington, Suite 190
Houston, TX 77043
(800) 225-2102

DATA I/O Corp.
10525 Williams Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 867-6899

GTEK, Inc.
P.O. Box 2310
Bay St. Lewis, MS 39521-2310
(800) 282-4835

Logical Devices, Inc.
1201 Northwest 65th Place
Ft. Lauderdale, FL 33309
(305) 974-0967

Logical Systems
P.O. Box 6184
Syracuse, NY 13217-6184
(315) 478-0722

Needham's Electronics
4535 Orange Grove Ave.
Sacramento, CA 95841
(916) 924-8037

North Valley Products
P.O. Box 32889
San Jose, CA 95152
(408) 929-5345

Stag Microsystems
528-5 Weddell Drive
Sunnyvale, CA 94086
(408) 988-1118

Z180, HD64180

8-BIT CMOS

AVAILABILITY: Now for 6-, 8-, and 10-MHz parts.

COST: For 10-MHz Z180, $12 (100) and $8 (1000). For 6-MHz HD64180, $7 (100) and $6 (1000).

SECOND SOURCE: None.

CORE: Zilog and Hitachi consider the basic Z180 and 64180 a standard cell for building high-integration µPs and µCs.

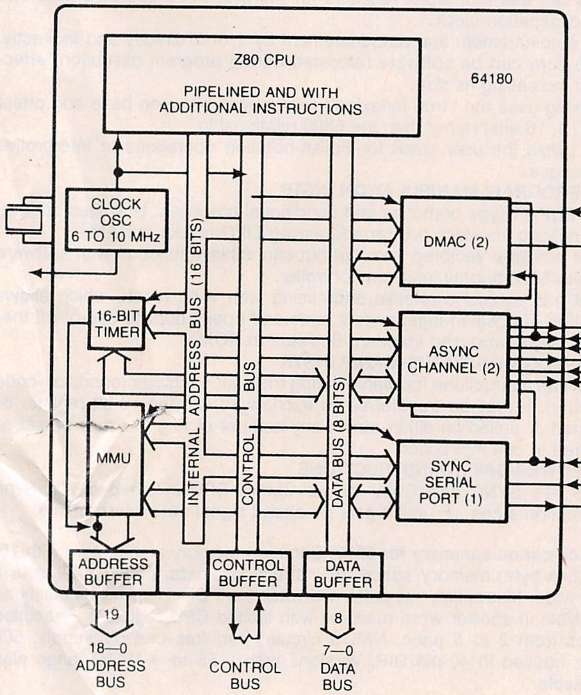
Description: Jointly developed enhancement of Z80 with various peripheral functions such as memory management (to reach larger, 1M-byte memory space), 2 DMA channels, 2 serial ports, and timers added on CMOS CPU chip. Z-suffix versions are totally compatible with Z80-family peripherals chips. Both Z- and R-suffix devices interface to the 6800 and Intel 80xx series buses.

Status: CMOS enhancements to the widely used Z80. Has on-chip memory-management unit (MMU), multiple DMA channels, and UART. These chips don't have sophisticated big-computer features, such as separate privileged "system" control registers, nor do they have a cache. Both the Z180 and 64180's MMUs translate between the Z80 64k-byte address space and their own 1M-byte space. These families have received a boost from all Z80 users and third-party supporters of the venerable Z80.

Zilog Inc
Intelligent Peripheral Controller Product Line
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000
For more information, Circle No. 365

Hitachi America Ltd
Semiconductor and IC Div
2000 Sierra Point Pkwy
Brisbane, CA 94005
Phone (415) 589-8300
For more information, Circle No. 366

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS

Unsigned 8 × 8-bit = 16-bit multiply.

Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator.

II—DATA-MOVEMENT INSTRUCTIONS

Immediately addressed locations.

Block output to I/O. Must set up MMU bank registers to translate between 64k bytes of Z80 and 512k bytes external.

V—POWER-SAVING INSTRUCTIONS

Sleep command disconnects processor from clock. Interrupt or reset will reconnect.

Specification summary: Object-code compatible with Z80 (and 8080, 8085). Pipelined CPU. On-chip MMU generates 19 bits (512k bytes external physical address space) in the DIP package and 20 bits (1M byte external) in surface-mount packages. 2-channel direct-memory-access controller, 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (Z-suffixed versions are matched to Z80-family peripherals). CMOS versions provide 50 mW at 4-MHz operation; lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

Hardware notes:

1. Diagram is for basic core. Both Zilog and Hitachi are expanding upon this core.
2. The 647180x is a single-chip version of the 64180 and adds 16k bytes of one-time-programmable EPROM, 512 bytes of RAM, 54 I/O pins, a 16-bit timer, and a 6-channel analog comparator. It comes in 84-pin PLCCs, 80-pin flatpacks, and 90-pin shrink DIPs. Because of EPROM, Hitachi bills this style µC as a zero-turnaround-time part, saying it is cost-effective in volumes as great as 10k. Hitachi also sells the part in windowed 84-pin leadless chip carriers to aid development.

Software notes:

1. Only new instructions beyond Z80 instructions listed.
2. The MMU adds base registers to Z80 16-bit addresses to produce the 19-bit addresses needed externally.
3. Trap interrupt can be used both for catching undefined op codes and for letting users extend instruction set.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Zilog offers a Z180 and serial communications controller (SCC) applications board to test and evaluate the chips.

From Hitachi: ASE Adaptive System Emulator ($7000) plus H6805M01S, a 256k-byte memory board for use with IBM PC, HP6400, or DEC VAX as host. Real-time operation as fast as 8 MHz and real-time tracer buffer for 2048 machine cycles. All hardware lines are captured, and the trace is automatically disassembled.

From Others: American Automation AA 572-64180 real-time in-circuit emulator for use with the company's E2-PRO development host.

Hewlett-Packard and Tektronix offer support on their development systems and logic analyzers.

Contact suppliers for the many other third-party vendors.

Microtec Research (Santa Clara, CA) supplies macroassembler, utilities, Pascal, and C compilers (to run on IBM PC and DEC VAX hosts). Avocet (Rockport, ME) and Allen Ashley (Pasadena, CA) have announced IBM PC-based assemblers. Hitachi provides help so that the additional 64180 instructions can be treated as macros on a Z80 macroassembler. Boston Systems Office (Waltham, MA) offers a VAX-hosted assembler ($1200). Software compatible with CP/M (Digital Research) and MSX (Microsoft) operating systems (latter being result of project for Japanese market). American Automation has cross software to go with development hardware (assembler, C compiler, and debugger). Archimedes (San Francisco, CA) offers a C compiler ($995 for IBM PC; $3995 for MicroVAX; and $7995 for VAX).

6800/6802, 6809/6309

8-BIT NMOS AND CMOS

AVAILABILITY: Now.
COST: As with other mature µPs, costs have dropped, in this case to a couple of dollars per µP), except when a part is at end of its life, in which case prices might rise again.
SECOND SOURCE: Hitachi and SGS Thomson.

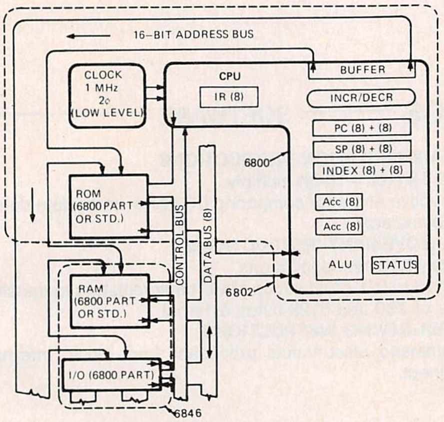
Description: The 8-bit 6800 CPU was the original part in the family named after it. That family has been broadened to include not only the 2-chip 6802/6846 and 6809 covered here but also the single-chip 6801, the low-end single-chip devices, and the 6804 and the 6805. Note, however, that new CPU members aren't precisely compatible with the original 6800, especially at the low and high ends. Even the 6809 is only software compatible with the original 6800 at source-code level.

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000
For more information, Circle No. 367

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest µP families. Among its progeny are the 6809 covered here and the following Motorola µPs and µCs, which are described elsewhere in this directory: the 6804, 6805, 6801, and 68HC11. The 6800 is now past its prime and is not recommended for new designs; we retain it in the directory for reference. But the newer 6802 and 6809 continue to be shipped in volume. For new designs, Motorola steers designers either upwards to the 16- and 32-bit 68000 family (68008 has an 8-bit bus) or downwards to the 68HC11.

CHARACTERISTICS

HARDWARE



Part	Description	Clock speed (MHz)	ROM ×(8)	RAM ×(8)	Cost (100 qty)
6800	CPU needs 2-phase clock	1–2	—	—	$4–$5
6802	CPU clock & RAM	1–2 (4-MHz ext)	—	128	$4–$5
6809	CPU	2	—	—	$5–$6
6309	CPU CMOS	3	—	—	$9.50

Hardware notes:
1. Diagram shows 6800 and 6802. The 6809 has another 16-bit index and a second "user" stack pointer, which make the 6809 more powerful than the 6800; these additional resources give the 6809 many more instructions. On simple benchmarks, the 6809 is 270% faster than the equivalent-speed 6800, programs in 42% fewer instructions, and uses 33% less code.
2. Basic 6809 version has on-chip clock. Minimum system results with the following parts: 6809, 6810, and 6846. 6809E version has off-chip clock. An early valid-memory-address (VMA) signal on 6809E allows 3-MHz bus operation with a 2-MHz memory. External clock permits multiprocessing.
3. The MMU (6829) allows the 6809 to run 32 concurrent protected tasks per management unit in a 2M-byte address space.
4. Hitachi CMOS version (6309) has 2-, 2.5-, and 3-MHz bus timing; the Sync and CWAI instructions allow a low-power sleep mode. Modify table from Nov 23, 1989, pg 130.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of two accumulators.
6809 has unsigned 8×8-bit multiply with 16-bit product.
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
6809 can use four index registers for merging three source blocks into one destination block.
Can autoincrement and autodecrement by 1 or 2 directly and indirectly.
Page zero can be software relocated during program execution, effectively increasing its size.
Indexing uses the "true indexing" relationship between base and offset (0, 5, 8, 16 bits) rather than the 6800 relationship.
Can utilize the user stack for Polish-notation operations or interpretive languages.
III—PROGRAM-MANIPULATION INSTR
Has PDP-11-type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM.
Does not have vectored interrupt but can achieve function with software or with 6828 priority interrupt controller.
6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs.
IV—PROGRAM-STATUS-MANIP INSTR
6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction.
V—POWER-SAVING INSTRUCTIONS
6309 has SYNC and CWAI to put CMOS CPU in sleep mode. Sync instruction stops µP until it gets go-ahead signal from interrupt line.

Specification summary for 6800: Common-memory architecture with 16-bit (64k-byte) memory space for instructions, data, and I/O; all data 8 bits wide. Instruction set patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 µsec. NMOS circuitry requires one 5V supply, 500 mW; housed in 40-pin DIP. Versions with −55 to +125°C range also available.

Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upwardly compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing increases throughput. Instruction set has 59 mnemonics and 7 addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-inherent operations executing in 1 µsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page-zero register is retained but can be software relocated anywhere in memory via programmable register. The chip requires one 5V supply. Two versions, each in 40-pin DIP.

SUPPORT

HARDWARE

From Motorola: Emulators range from low-cost (hundreds of dollars) boards to HDS-300 system (about $5000) plus personality modules ($5000).
Support systems and OEM boards available from Motorola Semiconductor Div, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-6900 or (602) 438-3500.
From others: Tektronix and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola's "Micromodule" 8-bit boards.

SOFTWARE

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 440-3733. The basic assemblers and other tools are for IBM PC.
Two versions of Basic are available for the 6809: Basic-M and Basic09. The latter is designed to be fast and to permit structured programming. A Pascal compiler diskette is available.

VGA

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ZL30A

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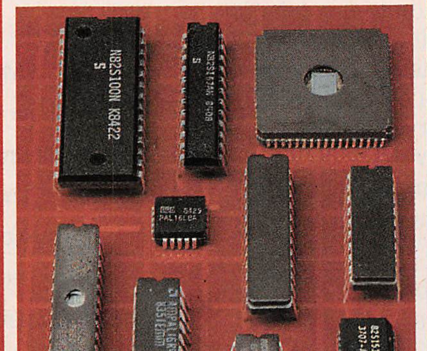

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Stag Microsystems, Inc.
1600 Wyatt Drive
Santa Clara, CA 95054

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Eastern Regional Office
Stag Microsystems, Inc.
3 Northern Blvd., Ste. B1
Amherst, NH 03031

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*CUPL is a trademark of Assisted Technology.

CIRCLE NO. 118

650X/65C0X

8-BIT NMOS AND CMOS

AVAILABILITY: Now.

COST: WDC's CMOS prices range from $4 in lower speed, high volume to $31.32 for high speed, lower volume.

SECOND SOURCE: WDC created and licensed most of the CMOS designs. It has licensed Rockwell, California Micro Devices, NCR, ITT-Intermetall in West Germany, and about 20 other companies.

CORE: WDC has developed the semicustom 6502 core as NCR and others now use it. Many suppliers now specify it as part of their cell libraries.

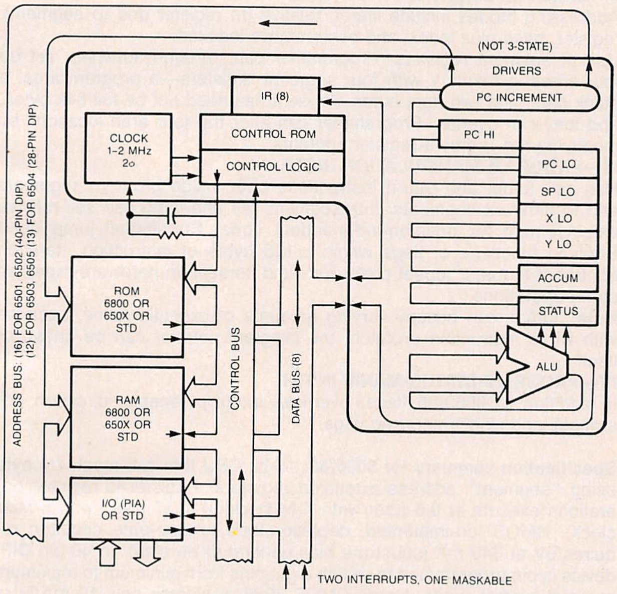
Description: Original design team's goal was to achieve as much PDP-11-style addressing capability as would fit in an economical chip. Because of the μP's short 8-bit index registers, it is optimally suited only to applications requiring access of smaller blocks of memory, although it benchmarks ahead of most other 8-bit μPs with respect to its speed of execution of high-level languages, such as Basic and Pascal. New CMOS parts consume little power and have small economical die that gets still smaller with today's finer geometries. See 6500/1 for single-chip versions and 65SC816/802 for 16-bit-internal version.

Originator of 6502 Commodore (Westchester, PA) no longer sells chips to the merchant market. WDC developed CMOS version.

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545
For more information, Circle No. 368

Status: The falling share of market for this μP appears to indicate that it has reached the end of its life cycle. However, the architecture lives on in the form of single-chip versions (see 6500/1 and especially the 50740 in this directory) and ASIC versions. Some of these have very large unit volumes, so the 6502 architecture may remain, by volume, the leading 8-bit architecture in the world.

HARDWARE — CHARACTERISTICS — SOFTWARE



Notes on CMOS versions:

1. CMOS 65CXX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are a new 4-phase clock that gives decreased memory access time and a memory-lock output and bus-enable input that simplify multiprocessor designs.
3. Among the software enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
4. Decimal mode is automatically set off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
5. A BRK followed by interrupt is executed.
6. See instruction set for comments on new instructions.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports. CMOS parts have bit manipulation.

II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, although index offset is limited to 8 bits in 2 CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables. CMOS parts have indexed-absolute indirect and zero-page indirect.

III—PROGRAM-MANIPULATION INSTR
Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model. CMOS parts have branches on bit test.
Stack pointer for implementing 256-byte LIFO in external RAM.

IV—PROGRAM-STATUS-MANIP INSTR
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits. 6502 and 6512 have external input to one status bit, useful for handshaking with peripherals.

V—POWER-SAVING INSTRUCTIONS
Wait and Stop on 65C02, respectively, stop processor and disconnect clock to lower power consumption. New operating voltage range of 1.2 to 5.25V with an I_{DD} of 0.1 μA/kHz at 2.8V.

Specification summary: Common-memory architecture with instructions, data, and I/O in same 64k-byte space; 57 instructions (68 for CMOS). Many instructions provide choice of 13 PDP-11-type addressing modes (15 for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mV supply. Some CMOS parts can run at 8-MHz clock frequency (125 nsec/cycle). CMOS parts require 4 mA/MHz for operation and 10 μW for standby. Although it supplies the μPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

HARDWARE — SUPPORT — SOFTWARE

From Rockwell: LCE emulator ($1250), which interfaces to IBM PC host. **Western Design Center** recommends using Hewlett-Packard (Colorado Springs, CO) logic analyzers.
From California Micro Devices: GEM-I ICE package ($3750) capable of interfacing with a variety of host computers including ISIS development system and Apple. Functions as a stand-alone assembler and disassembler using a nonintelligent terminal. Evaluation board for 65SC150 ($499) that functions as in-circuit system when coupled with GEM-I.
From NCR: Hardware emulator interfaces to Apple IIe through RS-232C port. Allows complete in-circuit software debugging.
From Dynatem (Irvine, CA): AIM-65 single-board computer and RM industrial modules.

From California Micro Devices: 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).
From NCR: Monitor for use in conjunction with emulator. Supports breakpoint, change memory and registers, software trace, and real-time execution.
From others: Because the 6500 has been so widely used, there are innumerable sources of software at different language levels: for example, Byte Works (Albuquerque, NM), S-C Software (Dallas, TX), Roger-Wagner Publishing (El Cajon, CA), and 2500 AD (Aurora, CO).

8086/8088

8/16-BIT NMOS AND CMOS

AVAILABILITY: Now.

COST: Under $10 (1000) for NMOS 8086/88, under $15 (1000) for CMOS 8086/88. Siemens' NMOS parts are under $4.50 (1000).

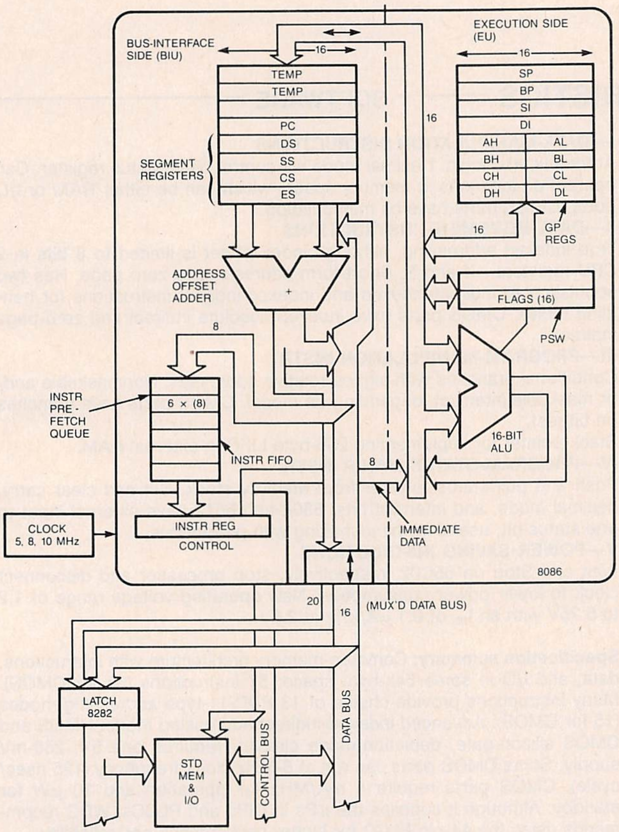
SECOND SOURCE: For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, and OKI.

Description: The 8086, 8088, and their low-power CMOS implementations (80C86/80C88) share a 16-bit internal architecture that has a software base of more than 10,000 DOS applications. The 8088 (used in the original IBM PC and its clones) has an 8-bit external data bus to allow the manufacture of lower cost systems with full 16-bit software capability.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 369

Status: Next to the 8080/Z80 family, the 8086 family has been the most successful µP family. Its most visible application has been in the IBM PC and its many clones.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:

1. Diagram is for initial family member, 8086.
2. 8088 is downgraded version of 8086. It has only 8-bit-wide external data output bus (only 8 lower bits of address bus are multiplexed for data). Some pin functions have been changed. Prefetch queue is only 4 bytes (to prevent overuse of bus). Instruction execution is slower because all 16-bit fetches and writes take 4 extra cycles.

I—DATA-MANIPULATION INSTRUCTIONS
8-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
Logicals.
Bit, byte, word, and block operations.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include literal, relative (to register and to segment), register, base-plus index, and base-relative indexed.
Use of segment registers: Programmer can, through software, set up four areas in memory with four segment registers—a program area, a stack area, and two data areas. These areas need not be full 64k bytes, and they can overlap. Programmer can alter the four area locations by modifying the segment-register contents.

III—PROGRAM-MANIPULATION INSTR
Has call, jump, and return instructions both inside program segments and to different segments. Intrasegment call and jump use self-relative displacement for position-independent code. Conditional jump upon Boolean functions of flags within ±128 bytes of instruction. Iteration control of loops, a repeat prefix for rapid iteration in hardware-repeated string operations.
Note: Jumps can occupy varying amounts of execution time, because with BIU's instruction prefetch, the program counter can be ahead of itself.

IV—PROGRAM-STATUS-MANIP INSTR
In addition to 8080/85 flags: overflow, interrupt enable, direction (for strings), and single-step trap flags.

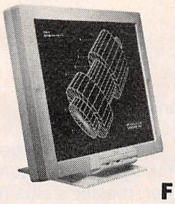
Specification summary for 8086/88: 16-bit CPU that can reach 1M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 µsec with 5-MHz clock (0.37 µsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry; requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch eight pins from minimum to maximum external system mode. Harris CMOS 8086 dissipates only 10 mA/MHz when running; clock can be stopped for 500 µA standby.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I^{2}ICE in-circuit emulator ($8495) supports 8086/8088 to 10 MHz. Emulators are hosted on IBM PC. All ICEs provide windowed, menu-driven, source-level display and µP debugging. Performance analysis tool (iPAT) consists of a hardware base unit, an interface to ICE, and host software for the IBM PC/XT and PC/AT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 8086/8088.
From others: Because of popularity, family is widely supported by third-party universal development systems.

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. DB-86 software debugger provides windowed, menu-driven, source-level debugging with full source-code display. Hosts include PC-DOS and VAX/VMS. Prices start at $750 (for DOS versions).
From others: Because of wide base of 8086/8088-based systems, particularly the IBM PC, there exists third-party software of all sorts, enough to fill whole catalogs. Check with Intel and various trade journals.

Panel of experts.



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It didn't take much research to discover what computer users in heavy-duty industrial, medical, and mainframe environments want from their displays. A bright, reliable, and interference-free picture.

To answer this need would take a lot more than a brilliant idea. It would take at least two.

Built to scale.

Idea number one is the very first 16-gray scale AC-memory plasma display available anywhere. An easy design-in, it interfaces with a standard Paradise™ VGA card to provide 640 x 480 pixels of flicker-free, high contrast viewing in even the toughest EMI environments. And that holds true for over 50,000 hours of continuous operation.

Product Selection Guide

Parts Nos.	Pixel/Format	Gray Scale	Screen Diag.
FPF8050HRUD-101	640 x 400	4	9″
FPF8050HRUK	640 x 400	4	10″
FPF8050HFUGA*	640 x 400	1	10″
FPF8060HRUM	640 x 480	1	10½″
FPF8060HRUK	640 x 480	4	10½″
FPF8060HRUS-120	640 x 480	16	10½″
FPF12896HRUF*	1024 x 768	1	15″
FPF128102HRUF*	1024 x 816	1	18″

*Also available as a monitor.

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Fujitsu Component of America, Inc.
3545 North First Street • San Jose, CA 95134-1804.

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CIRCLE NO. 70

Z280

8/16-BIT CMOS

AVAILABILITY: Now.

COST: About $18 in large volumes.

SECOND SOURCE: None announced, but supplier claims it has strong interest from major European and Far East semiconductor houses.

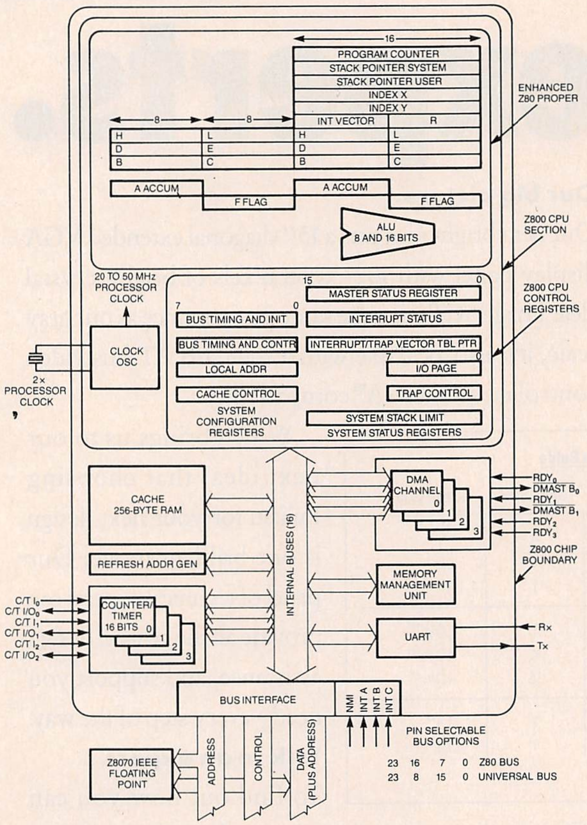
CORE: Zilog is incorporating elements of Z280 in its megacell library, so it can rapidly put together new combinations. The company claims it can turn around a semicustom design using its megacells in a matter of days. However, it does not plan to offer ASIC tools to customers.

Description: Enhanced Z80 µP, upgraded to the point that it has most of the features of larger 16/32-bit machines. It has "privileged" system-control hardware and associated software for multiuser, multitasking operating systems. It has memory management for virtual memory and incorporates cache to achieve high throughput with moderate-speed external memories.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000
For more information, Circle No. 370

Status: The Z280 became available in late 1987. Basically, the Z280 lets designers upgrade Z80-based PCs into multiuser systems that have large virtual memories and, claims Zilog, high performance. Compared with other Z80 enhancements, such as the Zilog Z180/Hitachi 64180, the Z280 offers a greater performance edge. Zilog is also pushing the Z280 as an upgrade for dedicated systems using Z80s as embedded controllers.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. The integration not only lowers system cost, but provides a speed advantage: When all subsystems are on chip, the system speed automatically increases.

I—DATA-MANIPULATION INSTRUCTIONS
16 × 16-bit = 32-bit multiply and 32/16-bit = 16-bit divide.
Extended block mode manipulates data in blocks.
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes for more general 16-bit use of Z80's 16-bit registers (HL, DE, BC pairs).
Instructions to communicate with coprocessors.
III—PROGRAM-MANIPULATION INSTR
Jump on auxiliary accumulator/flag.
Jump on auxiliary register file in use.
System call.
IV—PROGRAM-STATUS-MANIP INSTR
Master status register; see category V instructions.
V—SYSTEM CONTROL INSTRUCTIONS
Instructions for added system-control registers. These are privileged instructions to permit operating system to define the system configuration upon start-up, to use the new system stack pointer, master status register, and to set up the cache's operation mode.

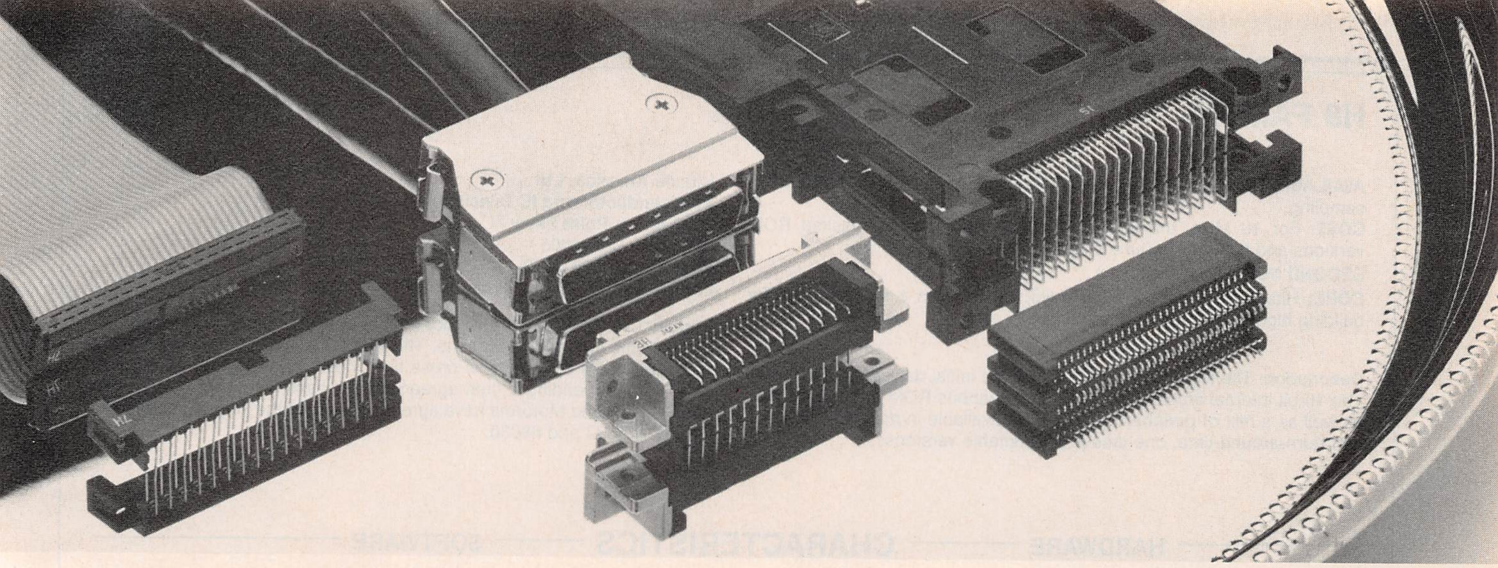
Specification summary: The Z80 is upwardly enhanced toward a general-register 16-bit minicomputer. On-chip memory management to address as many as 16M bytes of external memory. CPU is 3-stage pipelined with on-chip 256-byte program and data cache to automatically keep recently used instructions on chip for fast execution at 10-MHz internal bus clock. The I/O is pin programmable to match either 8-bit Z80 bus or 16-bit "universal" bus. Also included on chip are four 16-bit timer/counters, 4 DMA channel controllers, dynamic-memory refresh control, and a serial UART port. The Z280 will be fabricated in static CMOS and housed in 68-pin PLCC; other options planned for future as requested by customers.

Software note: Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Z280 Evaluation board.
From others: Softaid (Columbia, MD) has a low-cost real-time development system, and CDS ((704) 876-2346) offers evaluation boards for several popular buses. Logic analyzers are sold by Hewlett-Packard and Tektronix.

From Zilog: You can obtain a debug monitor program and a cross-assembler with Zilog's evaluation board. Zilog plans no other software support.
From others: 2500 AD is shipping a cross-assembler and is reported to be working on a C compiler. CDS offers both a cross-assembler and a C complier.



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Product Selection Guide

Series	Contacts	Current (ADC)	Part Nos.
FCN-210	30 to 120	2 (IDC: 0.5)	FCN-215Q050-G/O FCN-225J050-G/O
FCN-220 Card edge	30 to 120 (S-type: 112 to 187)	2	FCN-225J050-G/O
FCN-230	34 to 68	2 (IDC: 1)	FCN-235P048-G/O FCN-237J050-G/O
FCN-560 PC card	38	L: 2 E, G, F: 1	FCN-565F038-G/O
FCN-790 Low profile	10 to 40	1	FCN-794-P010-G/O FCN-795-P010-G/O FCN-797-P010-G/O

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H8 FAMILY

8/16-BIT CMOS

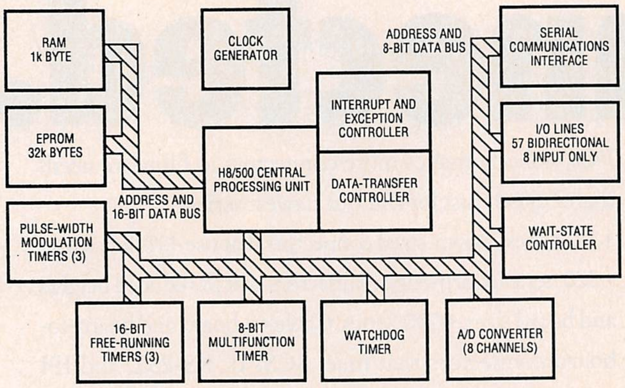
AVAILABILITY: Now for production quantities of the H8/532. H8/520 is sampling.
COST: For 10 MHz, the H8/532 costs $18 (10,000) in masked ROM versions and $25 for one-time programmable versions.
SECOND SOURCE: None.
CORE: Hitachi considers the basic H8/500 CPU as a standard cell for building high-integration μPs and μCs.

Description: The H8/532 and H8/520 are the initial devices in the family. The 16-bit internal architecture will include various ROM and RAM sizes, as well as a mix of peripherals. All will be available in masked ROM and zero-turn-around-time, one-time programmable versions.

Hitachi America, Ltd
Semiconductor and IC Division
2000 Sierra Point Pkwy
Brisbane, CA 94005
Phone (415) 589-8300
For more information, Circle No. 371

Status: The H8/532 is the vendor's highest performance microcontroller for real-time control applications. The H8/532 is involved in a legal battle with Motorola's 68030. As of press time, neither party has dropped current litigation pending a final agreement. However, to avoid delivery impact, Hitachi and Motorola have agreed to stays of the judgment concerning the H8/532 and 68030.

HARDWARE — CHARACTERISTICS — SOFTWARE


RAM
1k BYTE
CLOCK GENERATOR
ADDRESS AND 8-BIT DATA BUS
SERIAL COMMUNICATIONS INTERFACE
INTERRUPT AND EXCEPTION CONTROLLER
EPROM
32k BYTES
I/O LINES
57 BIDIRECTIONAL
8 INPUT ONLY
H8/500 CENTRAL PROCESSING UNIT
DATA-TRANSFER CONTROLLER
ADDRESS AND 16-BIT DATA BUS
PULSE-WIDTH MODULATION TIMERS (3)
WAIT-STATE CONTROLLER
16-BIT FREE-RUNNING TIMERS (3)
8-BIT MULTIFUNCTION TIMER
WATCHDOG TIMER
A/D CONVERTER (8 CHANNELS)

I—DATA-MANIPULATION INSTRUCTIONS
43 arithmetic, logic, shift, and bit manipulation instructions. Includes 16-bit multiply and divide.
II—DATA-MOVEMENT INSTRUCTIONS
7 data transfer instructions with high orthogonality. You can independently specify addressing modes and data sizes in each instruction. Seven addressing modes: register direct, indirect, indirect with displacement, indirect with pre-decrement or post-increment; absolute, immediate, and program-counter relative. Five data types: bit, BCD, byte, word, and long word.
III—PROGRAM-MANIPULATION INSTR
11 branch instructions with 16 different conditions. Loop counter/condition code register termination.
IV—PROGRAM-STATUS-MANIP INSTR
7 control registers including 16-bit program counter and status register; 8-bit condition code register, as well as four 8-bit page registers used in maximum mode only.
V—POWER-SAVING INSTRUCTIONS
3 Power-saving modes: sleep instruction halts CPU; sleep with software standby bit in control register set halts CPU and clock—a nonmaskable interrupt or hardware reset resumes execution; if standby pin is held low, processor enters hardware standby mode—a hardware reset resumes execution.

Specification summary: The H8/532 is an integrated 8-bit μC. Among the onboard peripherals are 32k bits of ROM or EPROM, 1k byte of RAM, 8 timers, 1 UART channel, 8 channels of 10-bit A/D conversion, 1 data transfer controller, 9 I/O ports, and glue logic that includes a clock generator and wait-state controller.

Hardware notes:
1. The H8/532 contains 32k bits of ROM and 1k bits of RAM. The chip offers a UART; three 16-bit free-run timers; an 8-bit timer; an 8-bit watchdog timer; an 8-channel, 10-bit ADC; and 3 external and 19 internal interrupts with 8 priority levels.
2. The H8/520 contains 16k bits of ROM and 512 bits of RAM. This chip features 2 UARTs. In addition to its two 16-bit free-run timers, the /520 offers both an 8-bit timer and a watchdog timer. This μC provides an ADC and interrupt structure like its sibling.

Software note:
Commonly used instructions have a short form: 1 byte shorter and executing 1 cycle faster than the corresponding long form.

HARDWARE — SUPPORT — SOFTWARE

Hitachi supplies a common base unit and personality modules for in-circuit emulation of all H-series devices (about $10,000). Evaluation boards (about $400) with in-line assembler and limited debug monitor are also available.
Hewlett-Packard (Palo Alto, CA) and Sophia Systems (Palo Alto, CA) also offer development systems.

Hitachi supplies a complete development software chain including assembler, linker, loader, simulator, and C compiler for VAX and IBM PC hosts. Third-party vendors Microtec Research (Santa Clara, CA), Avocet (Rockport, ME), and Software Environments (Dallas, TX) also supply similar products.

Touch down.

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Product Selection Guide

Series	Stroke	Tactile	Height (C-Row Center)
FKB7800	3.8mm	55gr	14.48mm
FKB8800	3.8mm	55gr	14.48mm
FKB4700	3.8mm	55gr	22.0mm*
FKB4800	3.8mm	55gr	22.0mm*

*without enclosure

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We hit the extra points.

Of course, what makes our new keyboards the best choice is what has made our FKB4800 and FKB4700 keyboards the 101 standard—our attention to the extra details. Like our superior tactile feedback and reliability

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CIRCLE NO. 72

78K SERIES

8/16-BIT CMOS

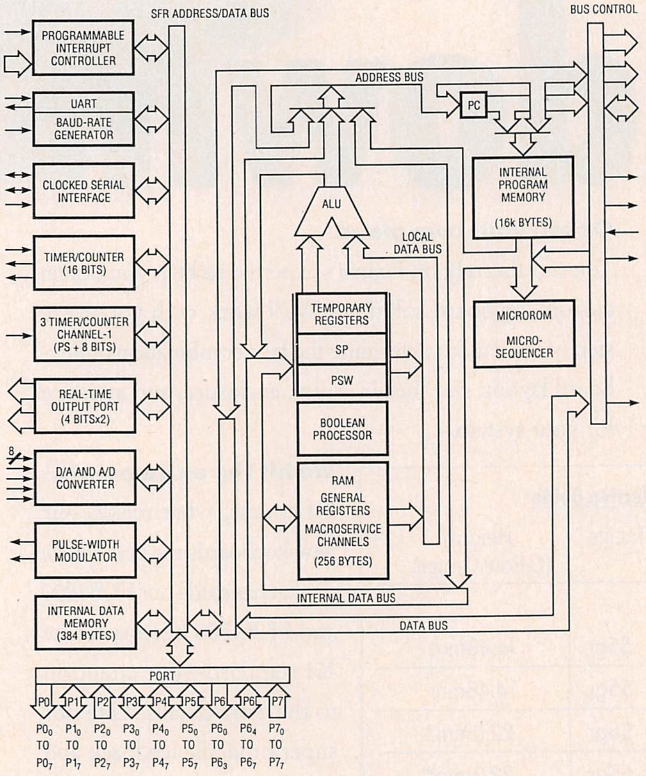
AVAILABILITY: Now.
COST: $5 - $10 (100,000).
SECOND SOURCE: None.

Description: The 78K Series is a family of 8/16-bit microcomputers with features for real-time applications. These µCs improve peripheral response and system speed while embedding intelligence in the peripherals and marrying the processor and peripherals through an interdevice data transfer facility.

NEC Electronics
401 Ellis St
Mountain View, CA 94043
Phone (415) 960-6000
For more information, Circle No. 372

Status: The K series of microcomputers is currently used in applications such as hard-disk drive control, audio, communication, and environmental control.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware note:
Diagram favors µPD7823x, which features synchronous and asynchronous serial I/O, counter/timers with compare and capture registers, multichannel ADCs, DACs, and a peripheral management unit.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, divide, logicals, compare.
II—DATA-MOVEMENT INSTRUCTIONS
Register-to-register moves. Load and store to external memory and I/O. Load and store multiple registers to and from external memory and I/O.
III—PROGRAM-MANIPULATION INSTR
Jump, call subroutine, and returns. Branches with decisions based on Boolean data in general-purpose registers rather than ALU condition codes.
IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition.
V—SYSTEM-LEVEL INSTRUCTIONS
Accumulator-oriented set, multiple register banks, condition flags.

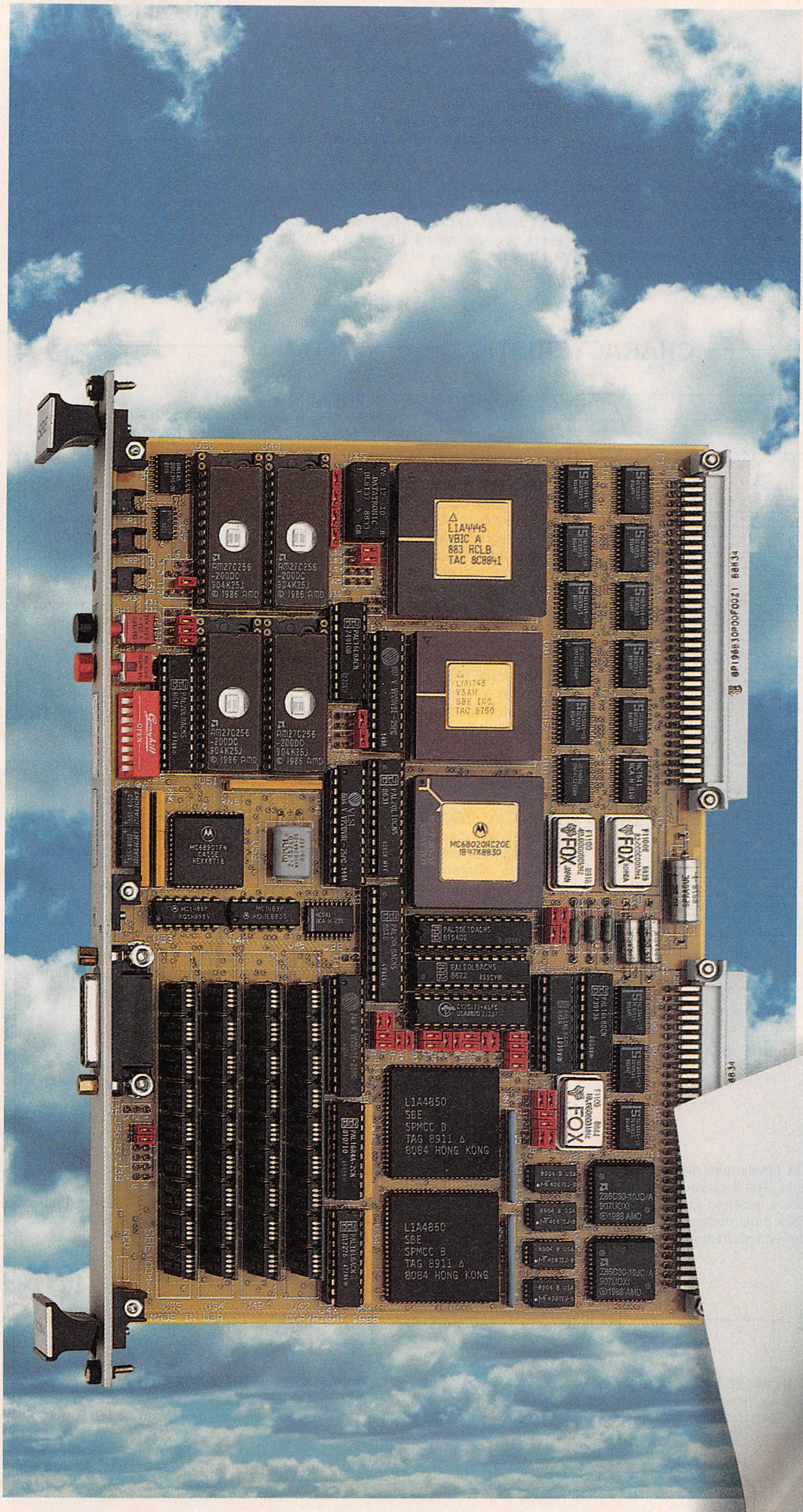
Specification summary: The intelligence of the peripheral management unit lets the chip handle many interrupt events without processor intervention. Instruction cycle times can be as long as 125 nsec at 32 MHz.

HARDWARE — SUPPORT — SOFTWARE

NEC Electronics provides an evaluation board with 32k bytes of RAM and ROM, an optional extended memory socket, and an RS-232C port. The Design kit includes a miniature-in-circuit emulator board and probe with 32k bytes of SRAM, a communications port, and an on-board monitor. The emulation kit includes ICE and probe.

In addition to support software for the development hardware, NEC provides a relocatable assembler, a structured assembler, and a C compiler.

For Versatile VME Solutions...Turn to SBE



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SBE

Communications & Real-time Solutions

CIRCLE NO. 124

65C816/65C802

8/16-BIT CMOS

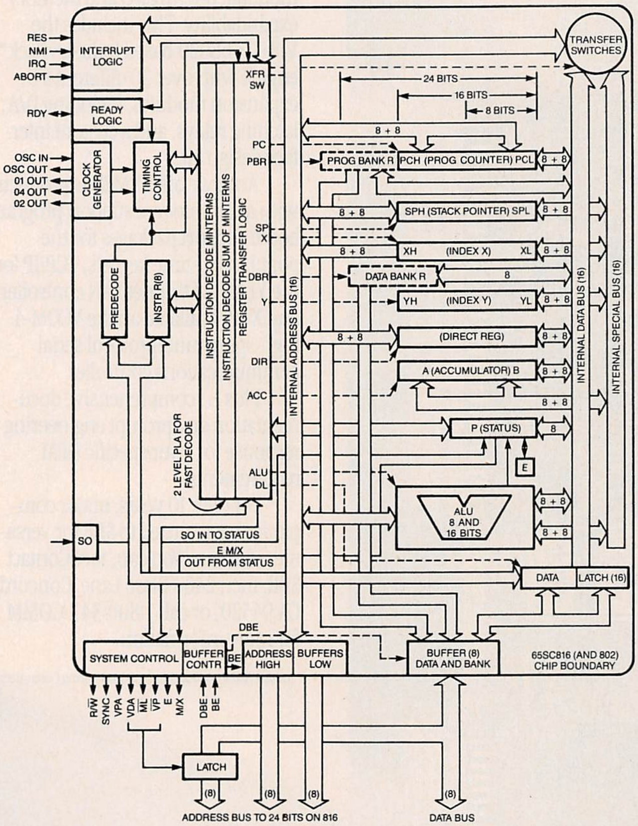
AVAILABILITY: Now.
COST: Prices range from about $4 to $32.
SECOND SOURCE: VLSI and California Micro Devices said to be main sources, but WDC says it has licensed others in US and abroad.
CORE: All suppliers are considering this as a μP megacell in their libraries.

Description: CMOS 8/16-bit μPs featuring software compatibility with 8-bit 6502 (both original NMOS 6502 and enhanced CMOS 65C02). The -802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The -816 has a different pinout, but expands the addressing range of the 6502 from 64k to 16M bytes. Additional hardware enhancements on the -816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545
For more information, Circle No. 373

Status: Apple's use of the 65C816 in the IIGS upgrade provides a firm basis for hardware and software availability. Software support is growing as third-party houses that have supported the 6502-based Apple computers convert software to take advantage of the expanded memory and other capabilities of the 65C816.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Compare diagram with previous 650X family (see diagram pg 127) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits, and the 16-bit registers widened to 24 bits.
2. The -816's control-bus outputs facilitate multiprocessing, caching, and virtual memory. The control-bus inputs let you abort instructions for virtual memory as well as control-bus access.

I—DATA-MANIPULATION INSTRUCTIONS
The 6502/65C02 instructions with 16-bit versions of add, subtract, BCD, and logicals. No multiply, but 65C832 version will have provisions for floating point on chip.
II—DATA-MOVEMENT INSTRUCTIONS
6502/65C02 instructions, but with choice of 8- or 16-bit indexing and 8-or 16-bit data widths.
On the -816, addressing can span 16M bytes with aid of paging through new register extensions. New block-move (forward or backward) instructions. Increased stack-pointer addressing modes, including stack relative, indirect, and indexed.
III—PROGRAM-MANIPULATION INSTR
Wait for interrupt and stop clock (restart via interrupt). Abort instruction on -816 via pin input acts as interrupt and directs program to perform memory repair and retry.
IV—PROGRAM-STATUS-MANIP INSTR
Additional bits in status register allow software selection of 8- or 16-bit modes for indexing and data. Also, E bit associated with status register (but not handled as part of it) provides software choice of emulation or native mode.

Specification summary: Enhanced 6502 with 16-bit internal data option and 24-bit addressing option, software selectable. Data I/O off chip remains 8 bits, however. The -802 version is hardware compatible with 6502 (or 65SC02) and can be plug-in replacement. It will reset into 6502 emulation mode, but can be software-switched into varying degrees of 16-bit operation. The -816 is almost identical internally to the -802, but it has different pinouts because it brings the additional bits for 24-bit address space out of the multiplexed 8-bit data-bus. The -816 also has special control lines to facilitate virtual memory, coprocessors, and data and program caching. Performance is mostly identical to 6502 of same clock speed, except that extended addressing and data modes take additional cycles. Clock to 12 MHz. Fabricated in 1.2-μm CMOS and features 3-mA/MHz power consumption, 1 μA in standby mode. Although it supplies the μPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

Software notes:
1. Upon reset, -802 and -816 are in 6502 emulation mode. To go to native (enhanced) mode, the E-bit must be reset to 0 via an exchange with previously reset carry-bit in status register.
2. Full-sized 16-bit registers may facilitate high-level-language compiler-writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help facilitate compiler writing. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Tendency of native (enhanced) mode coding to become trickier than 6502 due to tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

HARDWARE — SUPPORT — SOFTWARE

WDC recommends Hewlett-Packard (Colorado Springs, CO) logic analyzers to debug applications. HP offers several inverse assemblers for its logic analyzers. Microtek (Los Angeles, CA) and Macro Chip Research (Carrollton, TX) offer In-Circuit Emulators.

From Byte Works (Albuquerque, NM): The ORCA/M cross-assembly and utility package. C and Pascal compliers are also available.
From Apple (Cupertino, CA): Assembler and debugger ($100) and C compiler.
From others: Supporting products are also available from S-C Software (Dallas, TX); Roger-Wagner Publishing (El Cajon, CA); and 2500 AD (Aurora, CO).

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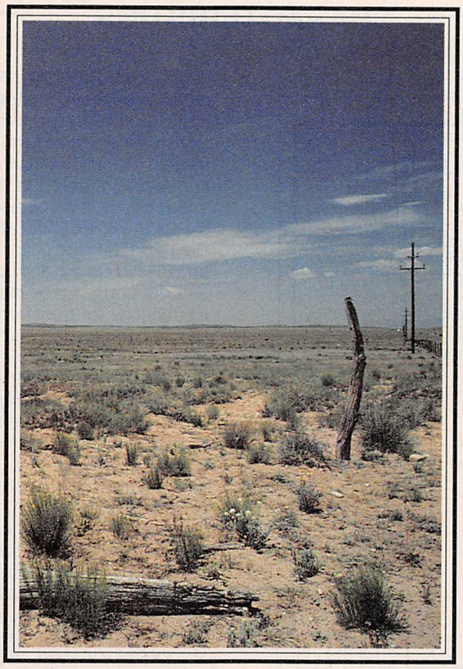

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Model	Speed (MHz)	Chips per set	Total IC's
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286/AT	12	3	8
286/AT	16/20	4	25
386SX/AT	16/20	2	12
386/AT	25/33	5	13/30
486/AT	40	—	—

Not including CPU, DRAM, EPROM, and keyboard decoder.

UMC

UNITED MICROELECTRONICS CORPORATION

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CIRCLE NO. 138

80186/80188

8/16-BIT NMOS AND CMOS

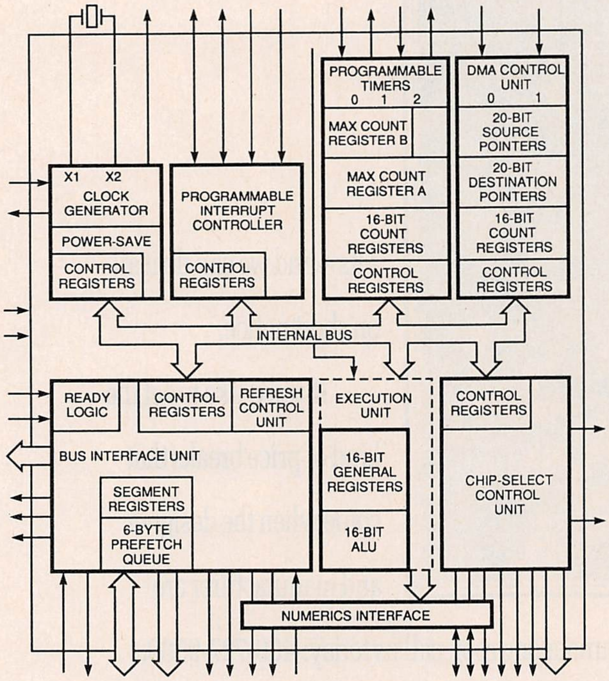
AVAILABILITY: Now for 8-MHz 80186/188. Now for 10-, 12.5-, and 16-MHz 80C186/80C188. AMD will have 20-MHz part in fourth quarter 1990.
COST: Less than $10 (100) for 80186/188 in PLCC. Less than $18 for 10-MHz 80C186/C188 in PLCC.
SECOND SOURCE: AMD and Siemens.
CORE: Intel's ASIC group has incorporated the 80C186 in its cell library.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 374

Description: The 80186, 80188, 80C186, and 80C188 are high-performance, highly integrated μPs. The 80186 family is completely upward compatible with 8086 object-code and contain 10 additional instructions. These embedded μPs integrate many common system components onto a single chip. The onboard peripherals include a clock generator, 2 independent DMA channels, a programmable interrupt controller, 3 programmable 16-bit timers, programmable memory, peripheral chip-select logic, and a programmable wait-state generator. Further enhancements to 80C186/C188 products include a fully static CMOS design, power-save mode, a DRAM-refresh control unit, a direct numerics interface, and a compatible mode.

Status: The 80C186 family of products is used in more than 3500 different customer applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram is for 80C186.
2. The 80C188 is the 8-bit external-data-bus version of the 80C186. The 80C188 has all other 80C186 features except for the numerics interface.
3. The 80186 and 80188 do not have the DRAM-refresh control unit, power-save mode, or the direct numerics interface.
4. The 8087 math coprocessor supports the 80186/188; the 80C187 supports the 80C186.

I—DATA-MANIPULATION INSTRUCTIONS
Includes addition, subtraction, multiplication, and division. Arithmetic operations may be performed on 4 types of numbers: unsigned binary, signed binary (integers), unsigned packed decimal, and unsigned unpacked decimal. Binary numbers may be 8 or 16 bits long. Decimal numbers are stored in bytes: 2 digits per byte for packed decimal, and 1 digit per byte for unpacked decimal.

II—DATA-MOVEMENT INSTRUCTIONS
Data-transfer instructions move single bytes, words, and double words between memory and registers, as well as between register AL or AX and I/O ports. Stack manipulation instructions are also included, as are instructions for transferring flag contents and for loading segment registers. Subgroups of the data transfer instructions are general-purpose data, I/O, address-object, and flag-transfer instructions.

III—PROGRAM-MANIPULATION INSTR
Includes unconditional transfers, conditional transfers, iteration controls, and interrupts. Unconditional transfers include call, jump, and return instructions, which may transfer control to a target instruction within the current code segment (intersegment transfer). The conditional transfer instructions are jumps that may or may not transfer control, depending on the state of the CPU flags at the time the instruction is executed. You can use the iteration control instructions to regulate the repetition of software loops. The interrupt instructions let programs, as well as external hardware devices, activate interrupt-service routines.

IV—PROGRAM-STATUS-MANIP INSTR
Flag operations include carry, direction, and interrupt enable, all of which let programs control various CPU functions.

V—SYSTEM-LEVEL INSTRUCTIONS
The processor controls instructions responsible for external synchronization, which include halt, wait, escape, and lock.

Specification summary: 16-bit CPU with direct-addressing capability to 1M-byte memory and 64k-byte I/O with 6 address modes. There are 14 16-bit registers. Register-to-register operations execute at 125 nsec for the 16-MHz device. The typical current for the 80186/188 at 5V is 320 mA; for the 80C186/C188 running at 16 MHz it is 105 mA. These parts come in 68-pin PGAs, LCCs, and PLCCs.

HARDWARE — SUPPORT — SOFTWARE

From Intel: I²ICE186 in-circuit emulator ($10,618) supports 80186 to 10 MHz. ICE186 in-circuit emulator ($15,995) supports 80186/80C186 to 16 MHz. I²ICE188 ($8495) and ICE 188 ($9995) support 8-bit bus versions of the 80186 (80188/80C188). An evaluation board is also available ($400).
From others: The family is widely supported by third-party universal development systems.

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. iPAT performance analysis tool enables the analysis of real-time software execution in prototype systems. Analysis is performed symbolically, nonintrusively, and in real time with 100% sampling in the μP prototype environment.
From others: Because of a wide range of 8086- and 8088-based systems, in particular the IBM PC, there is third-party software of all sorts, enough to fill catalogs. Check with Intel and various trade journals.

Text continued on pg 142

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Dallas Semiconductor	158-159
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Exar Corporation	1
Fujitsu Microelectronics	C2, 30, 129, 131, 133
Integrated Device Tech.	44
Intel	88-89
International Rectifier	C3
Linear Technology	139-140
Matra Harris Semi	216
Maxim Integrated Products	47, 49, 51
Micrel Semiconductor	146
Microlinear	194-195
Micron Technology	182
Motorola Semi	118, 58-59
National Semiconductors	142-144
NCR Corp.	176-177
NEC Electronics	185, 75, 76, 77
OKI Semi	24-25, 186
Precision Monolithics Inc.	164, 196
Samsung Semi	12-13
Siemens Components	
Signetics	22-23, 121-122
Silicon Systems Inc.	55
Sony Component Products	27, 74-75
Texas Instruments	34-37, 206-207
Zilog	81

CIRCLE NO. 30

80286

16-BIT NMOS

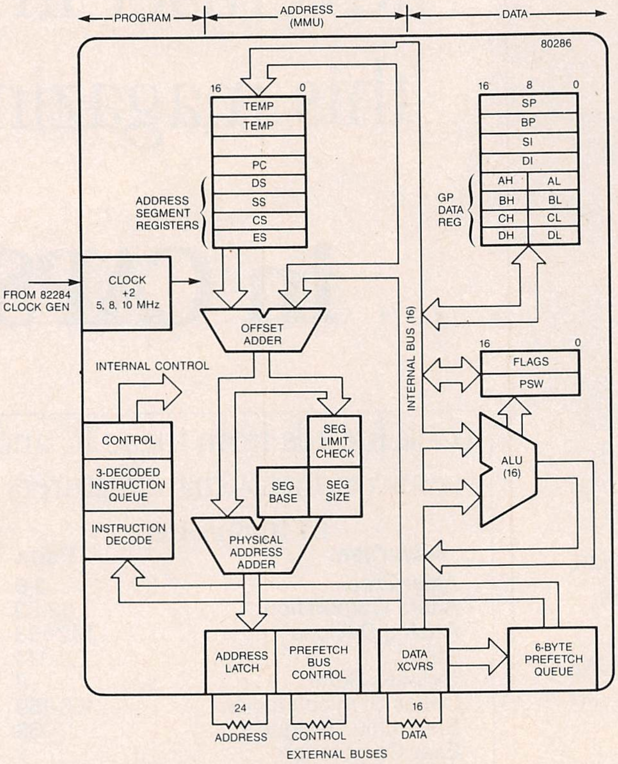
AVAILABILITY: Now for 8-, 10-, and 12.5-MHz devices. Now for 16- and 20-MHz versions from AMD and Harris. (Harris also offers a 25 MHz 80C286.) Now for CMOS 12.5-MHz 80C286.
COST: $10 (1000) for 8-MHz device; $13.50 (1000) for 12.5-MHz device. $30 (1000) for 12.5-MHz 80C286. Siemens charges $8, $12, and $21 (1000) for 8-, 12.5-, and 16-MHz devices, respectively.
SECOND SOURCE: AMD and Siemens. Harris for CMOS 80C286.

Description: The 80286 is upward compatible with the 8086 and 80188 and includes on-chip memory management and hardware support for multiuser, multitasking systems. A 4-level protection model provides task/task and user/operating-system protection. The 8-MHz 80286 is 6 times faster than the 5-MHz 8086 due to its pipelined architecture, 8M-byte/sec bus and 3.5-nsec interrupt time. Used in the IBM PC/AT and its clones.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 375

Status: Intel has de-emphasized the 80286 in favor of its 32-bit siblings, the 80386SX, 80386, and 80486. However, in spite of very low growth, the 80286 still has the highest volume in the 8086 family. Its popularity has been based on the IBM PC/AT. Since Intel has shown no inclination to let vendors second source the 80386, the 80286 should have a long life. Therefore, expect more enhanced 80286s, such as the 16- and 20-MHz versions from AMD and the CMOS version from Harris. Unfortunately for the second sources, the 80286's big sisters, the 80386SX, 80386, and 80486, are taking over many of its applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS

8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
Logical operations on bytes, words, and blocks.

II—DATA-MOVEMENT INSTRUCTIONS

Addressing modes include literal, relative (to register and to segment), register, base plus index, base relative indexed, and register indirect.
Programmers can manipulate 16,383 segments in memory by means of memory-base descriptor tables and 4-segment registers. These segments can be between 1k and 64k bytes in length.

III—PROGRAM-MANIPULATION INSTR

Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks.
Intrasegment calls and jumps use self-relative displacement for position-independent code.
Intersegment calls and jumps use the memory-based descriptor tables to provide position independence of code.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.
String instructions, including repeat, for rapid iteration.

IV—PROGRAM-STATUS-MANIP INSTR

8085 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible.

Specification summary: 16-bit CPU with 1G-byte virtual-address space per user, mapped onto 16M-byte physical-address space. Bus cycles execute in 250 nsec at 8-MHz clock frequency (200 nsec at 10 MHz), requiring 0.25 μsec for register-to-register moves at 8-MHz clock frequency, with 8M-byte/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry in a large chip (335×339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has 2 operating modes: Real-address mode emulates 8086; protected virtual-address mode native to 80286. Housed in a 68-pin Jedec type-A LCC, PLCC, and PGA.

Hardware notes:
1. Support chips for 80286: 82C284 clock, 82288 bus controller, 80287 floating-point numeric processor ($187.15 (1000) for 10-MHz version), and 82258 advanced DMA coprocessor.
2. High-integration chip sets for the IBM PC/AT are being offered by Chips and Technologies (San Jose, CA), Zymos (Sunnyvale, CA), VLSI Technology (Phoenix, AZ), Hudson & Supinger (Santa Clara, CA), Capital Equipment Corp (Burlington, MA), and Via Technologies Inc (Sunnyvale, CA), as well as by Intel. These chips consolidate devices used around compute engines for the 80286.

Software notes:
1. Has high-level-language support instructions.
2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.
3. Trusted instructions can only be executed at highest protection levels.

HARDWARE — SUPPORT — SOFTWARE

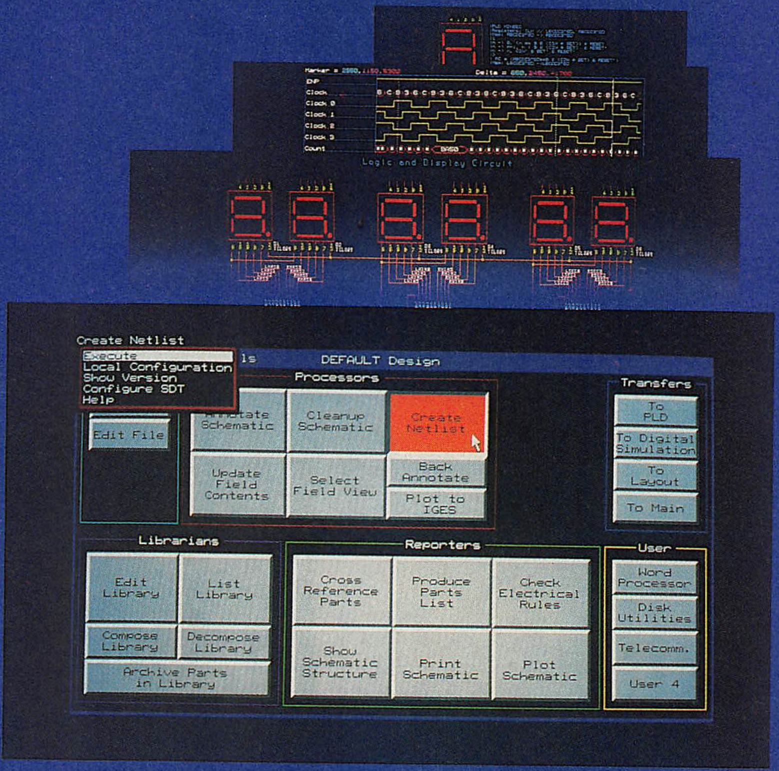
From Intel: I²ICE-286 in-circuit emulator ($12,494) supports 80286 at 8 and 10 MHz. It is hosted on IBM PC/AT and PC/XT. ICE286 ($12,495) supports 80286 at 12.5 MHz. iPAT performance analysis tool includes a hardware base unit, an interface to the in-circuit emulator, and host software for the PC/AT and PC/XT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 80286 in real and protected mode.
From others: A number of third-parties support the 80286 on their universal development systems.

From Intel: Macroassembler (ASM 286), which includes systems builder, binder, mapper, and librarian. Compilers for C, Pascal, PL/M, and Fortran. For applications running in virtual 8086 mode, any of Intel's 8086 software tools can be used. Hosts include PC-DOS and VAX/VMS. $750 for DOS version. Real-time operating systems (Intel's iRMX 286) available.
From others: Other operating systems and compilers being developed by third-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Coherent 286 (Mark Williams), Concurrent DOS (Digital Research), Unix System V (Digital Research), and OS/2 by Microsoft (Redmond, WA).

Text continued on pg 147

OrCAD presents

Release IV



The limits are gone

OrCAD has introduced the greatest product upgrade in its history. Memory limits, design restrictions, even boundaries between products are all disappearing.

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- Schematic Parts Library has been increased to over 20,000 unique library parts
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- Printed Circuit Board Layout package offers autoplacement and autorouting at no extra charge
- Expanded memory capabilities

Best of all, OrCAD introduces ESP

ESP is a graphical environment designed specifically for the electronic designer. Software tools appropriate for different stages in the design process are now linked together to form a seamless flow of information. This easy-to-use framework relieves the designer of time consuming tasks and the inconvenience of moving from one tool set to another. You can now spend more time productively designing.

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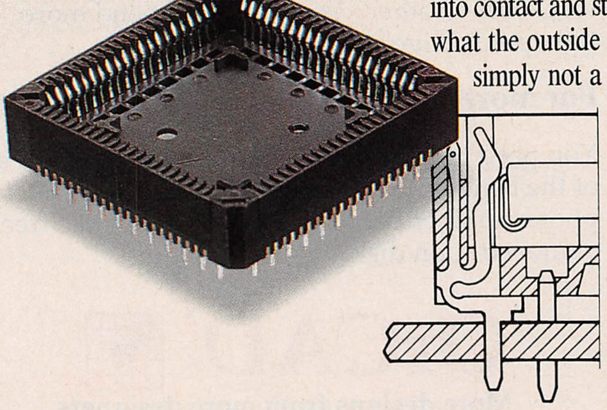
CIRCLE NO. 104

A chip carrier socket that won't play "pop goes the circuit."

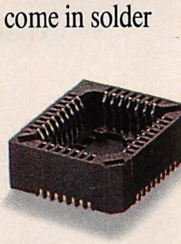


Our sockets are designed to get solidly into contact and stay in contact. No matter what the outside influences. Pop-out is simply not a problem.

Controlled contact interface angle in AMP HPT sockets ensures positive chip carrier retention. Our exclusive removable housing allows direct inspection of solder joints, and fast repair/replacement of contacts.

The contacts are High Pressure Tin, an AMP proprietary design which creates very high normal forces—a minimum of 200 grams per contact—for maximum retention and reliable interconnection. Short-signal-path contacts float in the housing to accommodate thermal expansion.

Two basic styles of sockets are available: square or 32-position rectangular EPROM and SO-J. Both come in solder



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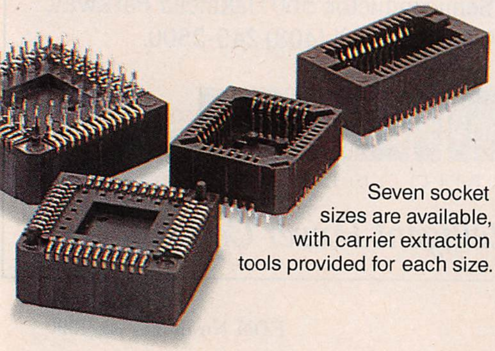
tail or surface mount versions and feature all the important details. Tin-over-nickel plating is applied after the contacts are formed, to assure full plating. We've built in visual indicators for locating pin 1, and polarizing to aid correct insertion.

Orientation holes in the 94V-0 housing floor make registration to the pc board both fast and simple, ideal for hand or tube-loaded robotic insertion. And the high pin counts make very effective use of real estate.

Call the AMP Information Center at 1-800-522-6752 for literature on HPT PLCC Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

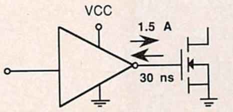
AMP Interconnecting ideas



Seven socket sizes are available, with carrier extraction tools provided for each size.

Now, one family drives all FETs.

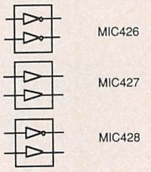
High Speed, High Current Low Side MOSFET Drivers

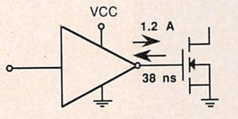


Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC426/7/8 (Original)

- 30 nS into 1000 pF
- 4.5 V to 18 V supply
- 1.5 A peak output
- 6 Ω output impedance
- Available in surface mount packages

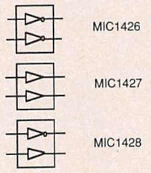


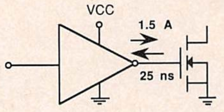


Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC1426/7/8 (Low Cost)

- Low cost predriver
- 38 nS into 1000 pF
- 4.75 V to 16 V supply
- 1.2 A peak output
- 8 Ω output impedance
- Available in surface mount packages

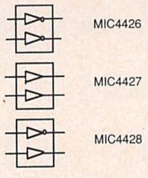


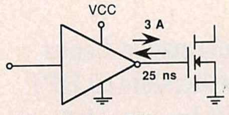


Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC4426/7/8 (Protected)

- Latch-up protected
- 25 nS into 1000 pF
- 4.5 V to 18 V supply
- 1.5 A peak output
- 7 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount and high temperature packages

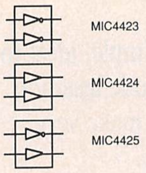


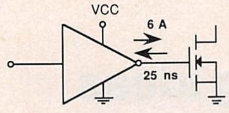


Drives a hex 4 - hex 5 size MOSFET; 6000 pF to 12000 pF.

MIC4423/4/5 (High Current)

- Latch-up protected
- 25 nS into 1800 pF
- 4.5 V to 18 V supply
- 3 A peak output
- 3.5 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount packages

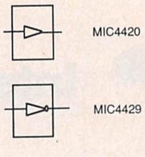


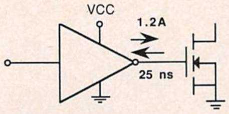


Drives a hex 6 - hex 7 size MOSFET ; 15000 pFto 16000 pF

MIC4420/4429 (Singles)

- Latch-up protected
- 25 nS into 10,000 pF
- 4.5 V to 18 V supply
- 6 A peak output
- 2.5 Ω output impedance
- Withstands 5 V negative swing
- Available in surface mount packages

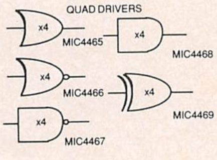




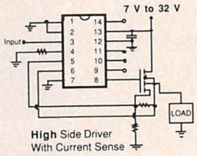
Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF

MIC4465/6/7/8/9 (Quad)

- Latch-up protected
- 25 nS into 470 pF
- 4.5 V to 18 V supply
- 1.2 A peak output
- Available in surface mount packages
- Five logic choices



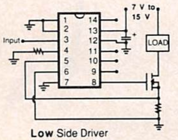
High Side, Protected MOSFET Drivers



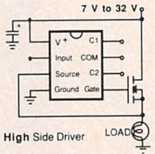
High Side Driver
With Current Sense

MIC5010

- Full Featured predriver
- Optional speed up caps
- 7 V to 32 V supply
- Internal charge pump
- 60 µS into 1 nF
- Over current sensing
- Fault flag output
- Surface mount packages
- Dynamic sensing threshold



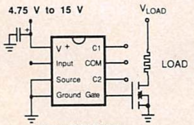
Low Side Driver
With Current Sense



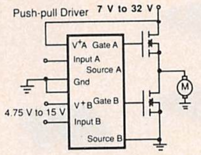
High Side Driver

MIC5011

- Minimum parts count
- Optional speed up caps
- 4.75 V to 32 V supply
- Internal charge pump
- 60 µS into 1 nF
- Surface mount packages

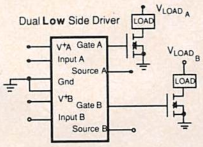


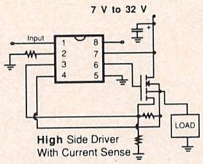
Low Side Driver



MIC5012

- Dual predriver
- Provides high and low side
- 4.75 V to 32 V supply
- Internal charge pump
- 60 µS into 1 nF
- Surface mount packages

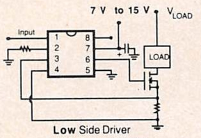




High Side Driver
With Current Sense

MIC5013

- Over current sensing
- 7 V to 32 V supply
- Fault flag output
- Internal charge pump
- 60 µS into 1 nF
- Surface mount packages
- Dynamic sensing threshold



Low Side Driver
With Current Sense

Choose from the widest selection of MOSFET predrivers in the industry. Whether your specification requires ultrafast low side driving, overcurrent protected high side driving, or overcurrent protected low side driving of 1 Amp to 100 Amp MOSFETs, we can supply the right product from our family of CMOS drivers to reliably meet your needs. For details contact: Micrel Semiconductor, 560 Oakmead Parkway, Sunnyvale, CA 94086. Or call (408) 245-2500.

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MCS-96 FAMILY

16-BIT NMOS AND CMOS

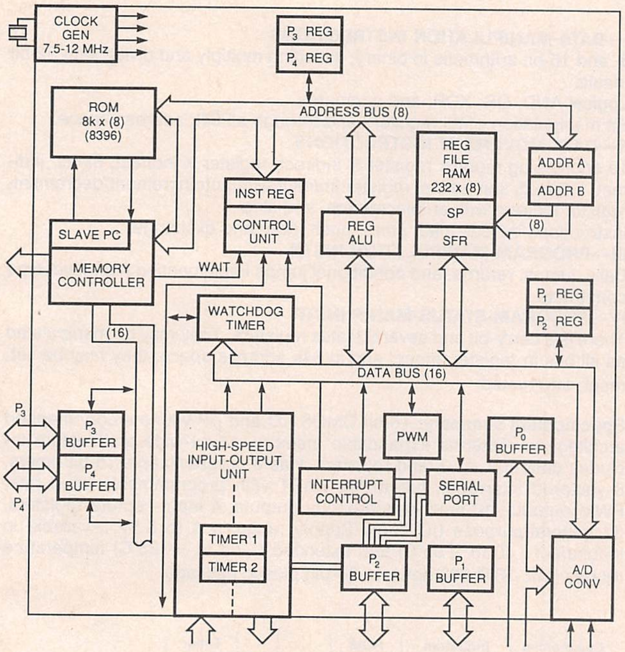
AVAILABILITY: Now for 8096BH, 8097BH, 8097JF, and 8098.
COST: $5-$20.
SECOND SOURCE: None.

Description: Highly integrated 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes as much as 8k bytes of ROM/EPROM/OTP and 232 bytes of register-file. Also includes as much as 256 bytes of on-chip code RAM. I/O capabilities include an 8-channel, 10-bit ADC, full-duplex UART, 8-level priority interrupt, pulse-width-modulated output, high-speed I/O subsystem, four 16-bit software timers, as many as five 8-bit I/O ports, and 1 watchdog timer.

Intel Corp
Chandler Microcontroller and ASIC Div
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 376

Status: This earliest of the 16-bit μCs continues to maintain a large share of the 16-bit market. Intel has expanded the MCS-96 family to suit various segments of the market.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide.
Logicals.
Bit, byte, word, and double-word operations.
II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include direct, immediate, indexed, indirect, and indirect with autoincrement.
Load and store, push and pop.
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.
IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, and sticky bit (records previous value of carry during right shifts).
Can set and clear some bits.

Specification summary: 16-bit μC with split-memory architecture; 8k-byte ROM and 232 bytes of register-file RAM on chip. External memory expandable to 64k bytes, with data-bus dynamically programmable as 8 or 16 bits. Register-to-register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter; four 16-bit software timers; PWM output; five 8-bit I/O ports; full-duplex serial port; and high-speed pulse I/O ports. 16×16-bit multiply as fast as 1.75 μsec and 32/16-bit divide as fast as 3 μsec. In 48-pin DIP, 68-pin PLCC, or 68-pin PGA.

Hardware notes:
1. The NMOS MCS-96 family consists of parts available with A/D converter, 8- or 16- bit external bus. On-chip memory alternatives include ROM, EPROM, and one-time programmable versions. Packaging options include 68-pin PLCCs, 64-pin shrink DIPs, 48-pin DIPs, and 68-pin PGAs.
2. I/O subsystem has 4 high-speed capture inputs and 6 high-speed pulse outputs. Storage in 8-deep FIFO (inputs) and content addressable memory (outputs).
3. 16-bit watchdog timer allows recovery from hardware or software error.

HARDWARE — SUPPORT — SOFTWARE

Programming support for EPROM versions supplied through Intel's line of universal PROM programmers as well as third-party programs from companies such as Data I/O, Stag, and Elan.
From Intel: Macroassembler (ASM-96), PL/M-96, and C-96 compilers. PL/M and C compilers supply hardware-control features such as interrupts. Each software package includes relocation/linkage utility (RL-96); library management utility (LIB-96); object-to-hex conversion utility (OH-96); and FPAL-96, a 32-bit floating-point utility. Software packages run on IBM PCs and compatible computers. $750 for a single-user license.

From Archimedes (San Francisco, CA): ANSI C-8096 compiler with additional features, such as control of interrupt. Hosted on IBM PC ($995), MicroVAX ($3995), and VAX ($5995).
From Cybernetic Micro Systems (San Gregorio, CA): Graphics programming and simulation aids, which run on IBM PCs ($295 and $995, respectively).

HPC16000 FAMILY

16-BIT CMOS

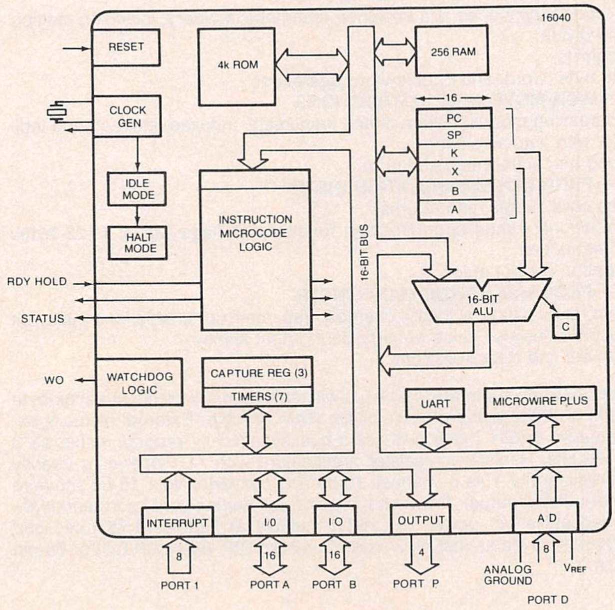
AVAILABILITY: Now for 20- and 30-MHz parts.
COST: $5 to $25 in volume.
SECOND SOURCE: None.
CORE: The HPC family is core based. National says the family of standard parts is continuously growing.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000
For more information, Circle No. 377

Description: 16-bit CMOS µC family with basic version having onboard ROM, RAM, extensive I/O, and peripherals. Original HPC had 16.8-MHz clock. Due to shrinking, new HPC16083 is offered in both 20-MHz and 30-MHz versions. The 30-MHz part's shortest instructions are just 134 nsec over −55 to +125°C.

Status: HPC is a family of industrial controllers. Supplier's benchmarks (August '86 with HPC at 17 MHz) indicate that HPCs out perform other similar 8- and 16-bit controllers, such as Intel 8096, Motorola 68HC11, and TI370 on both throughput and ROM-program efficiency. NEC 78XXX and Zilog Super Z8 weren't mentioned. Dataquest numbers show the HPC as the largest selling 16-bit CMOS µC.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Family is designed around common µP core for instruction-set consistency, with different models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are ADCs, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPROMs.
2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (ADCs, display drivers, EEPROM), COPS 4-bit µCs, 8050 8-bit µCs, and other HPCs for multiprocessing.
3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity, such as infinite loops.
4. Halt and idle modes provide additional power savings by stopping clock or disconnecting it.
5. Emulator parts are available for the HPC family.
6. HPC16083 and HPC16003 are MIL-883 and DESC-qualified.

I—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results.
Logical AND, OR, XOR, and compares.
Bit manipulation of all registers and through all 64k address space.
II—DATA-MOVEMENT INSTRUCTIONS
10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip.
Instructions include load, store, push, pop, and exchange.
III—PROGRAM-MANIPULATION INSTR
Calls, jumps, returns, and conditional jumps implementing high-level-type constructs.
IV—PROGRAM-STATUS-MANIP INSTR
There is a carry-bit and several status registers. They may be manipulated as all bits in register space, and in 64k address space, they may be set, reset, and tested.

Specification summary: 16-bit CMOS µC and µP with memory-mapped architecture. External expandable memory. 16-bit-wide architecture includes data bus, ALU, and registers. Has 8 programmable 16-bit timers, 8 vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, 4 input-capture registers, 52 general-purpose I/O lines. Supply range is 4 to 5.5V. Available in industrial (−40 to +85°C) and extended (−55 to +125°C) temperature ranges (MIL-STD-883 now). In 68-pin plastic package.

Commercial version (0 to 70°C)	Industrial version (−40 to +85°C)	ROM EPROM (bytes)	RAM (bytes)	I/O pins	Timer base counters	Other
HPC46003	HPC36003	ROMless	256	52	8	4 input capture registers
HPC46004	HPC36004	ROMless	512	52	8	4 input capture registers
HPC46064	HPC36064	16.0k	512	52	8	4 input capture registers
HPC46083	HPC36083	8.0k	256	52	8	4 input capture registers
HPC46104*	HPC36104	ROMless	512	52	8	4 input capture registers and 8-channel ADC
HPC46164*	HPC36164	16.0k	512	52	8	4 input capture registers and 8-channel ADC
HPC46400	HPC36400	N/A	256	56	4	HDLC & DMA
HPC46400	HPC36400E	N/A	256	56	4	HDLC & DMA
HPC467164*	HPC367164	16.0k	512	52	8	EPROM & one-time-programmable device
HPC46083MH		8.0k	256	52	8	EPROM

*Available in 1991
All devices have 8 interrupts, implement their stacks in RAM, have at least 1 serial I/O port, and come in 68-pin packages
MIL versions available

HARDWARE — SUPPORT — SOFTWARE

A designer's kit is available for less than $500. Supplier's HPC development system costs approximately $7000 for the HPC family. A high-end development system will be available from Hewlett-Packard as part of the HPC64700 in 1990. Both development systems can be used in conjunction with various hosts like IBM PC/ATs or HP9000 Series 300s.
Dial-A-Helper is a 24-hr, on-line computer bulletin board serviced by National. It provides the latest information on all National µC chips (including development systems) and also specific application support. Call (408) 739-5582 for more information.

Cross-assembler and C compiler to run on IBM PC. VAX (Unix/VMS) support is available, as is a symbolic debugger. Floating-point math and general math packages are currently available. Extensive application software is available for ISDN and SCSI.

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1985
TLC549
8 Bit A/D
Introduction of LinCMOS Technology

1986
TLC1540
10 Bit A/D
12 Channel LinCMOS Technology

1987
TLC7524 (AD7524)
1st D/A Converter
Introduction of Advanced LinCMOS Technology

1987
TLC7528 (AD7528)
1st 8-bit D/A Dual Channel
Advanced LinCMOS Technology

1988
TLC10 (MF10)
1st Dual-switched Capacitor With Filter
Advanced LinCMOS Technology

1989
TLC32044
1st 14 Bit A/D, D/A And Filter On Same Chip
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CIRCLE NO. 100

80C166

16-BIT CMOS

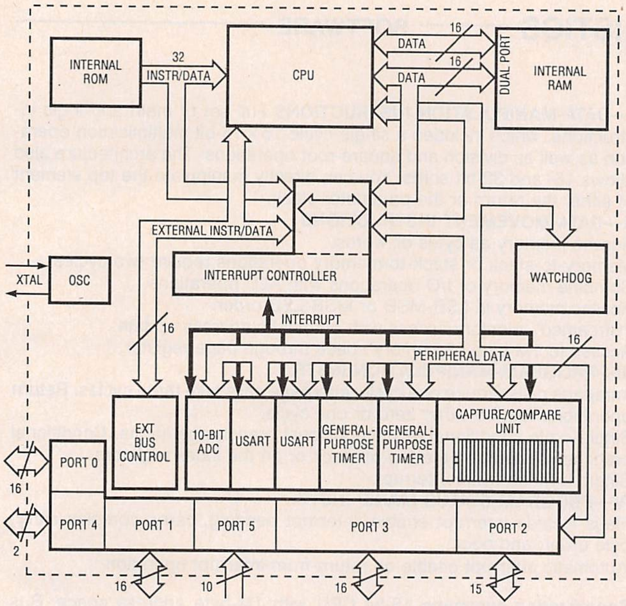
AVAILABILITY: Now.
COST: $25 (10,000)
SECOND SOURCE: SGS-Thomson.

Description: The 80C166/83C166 is a 16-bit microcontroller for real-time applications. It uses a pipelined architecture and performs 8-, 16-, and 32-bit arithmetic and bit, byte, and word manipulations. You can freely allocate, within the internal RAM, any number of register banks with as many as 16 general-purpose registers. An interrupt controller with a peripheral event controller provides fast response to external events.

Siemens Components Inc
Integrated Circuits Div
2191 Laurelwood Rd
Santa Clara, CA 95054
Phone (408) 980-4518
For more information, Circle No. 378

Status: Siemens claims its 16-bit modular design works well in automotive, industrial-control, and data communications applications. The 80C166 uses the vendor's experience with highly integrated derivatives of the 8051. Changing peripheral modules and on-chip RAM and ROM sizes to suit particular applications will help the family grow.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The peripheral event controller services peripherals independent from the CPU. This controller module acts as an interrupt-driven DMA function between the CPU and peripherals.
2. The 80C166 is a task-oriented machine. The programmable interrupt priorities, a number of hardware and software traps, fast interrupt response time, and programmable register-bank allocation allow fast task switches.

I—DATA-MANIPULATION INSTRUCTIONS
8-, 16-, and 32-bit signed and unsigned arithmetic instructions including fast multiply and divide. Multiple-bit shift and rotate in one machine cycle. Direct bit-to-bit manipulation in internal RAM. Various loop-control instructions.
II—DATA-MOVEMENT INSTRUCTIONS
Move instructions of byte or word in direct, immediate, indexed, and indirect with auto increment or decrement addressing modes. Flexible byte-to-word movements, system stack and user stack instructions.
III—PROGRAM-MANIPULATION INSTR
Intersegment and intrasegment calls and jumps. Conditional jumps on 16 different conditions (including semaphore support). Software traps.
IV—PROGRAM-STATUS-MANIP INSTR
You can change the current CPU priority to mask reactions on interrupts of lower priority. Hardware traps are issued on detected errors. A system-configuration register allows adjustment of the µP to various system requirements.

Specification summary: Single-chip microcontroller with external bus interface, as much as 32k bytes of ROM or flash EPROM, and 1k byte of RAM. Selectable 8- or 16-bit external data bus with programmable wait states or ready function. Chip uses 40-MHz crystal to run at 20 MHz. Most instructions execute in one machine cycle. Interrupt response takes 3 to 5 cycles. You can allocate 32 interrupt sources to 16 priority levels. The peripheral event controller steals cycles to implement fast, asynchronous data transmissions. The capture/compare unit consists of two 16-bit timers with 400-nsec resolution. A general-purpose timer unit contains three 16-bit up/down timer/counters with 400-nsec resolution. Another general-purpose timer unit offers two 16-bit up/down timer/counters with 200-nsec resolution. The 80C166 provides 76 I/O lines in four 16-bit bidirectional ports, one 2-bit bidirectional port, and a 10-bit input port. Two USART channels provide 625k-baud serial communication. An on-board ADC provides 10-bit resolution and 15-µsec conversion time.

HARDWARE — SUPPORT — SOFTWARE

Siemens supplies an 80C166 evaluation board with monitor and an emulator based on a bond-out chip. The board uses the IBM PC as a host.

From Siemens: A development package that includes a macro assembler, linker, locator, and library. A C compiler for ANSI standard C with additional support for 80C166-specific features. A software simulator that can simulate on-chip peripherals and an interrupt system allows debugging and software development. All software tools are IBM PC-based and are currently available.

RTX 2000

16-BIT CMOS

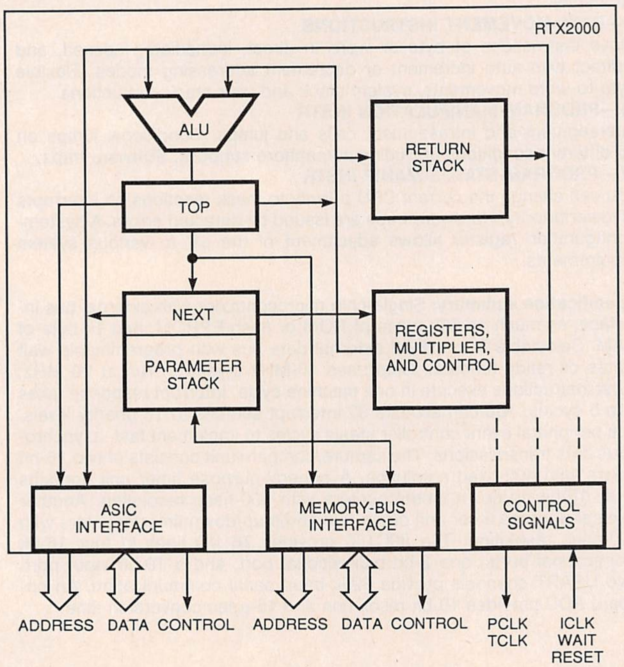
AVAILABILITY: The RTX 2000-8 (8 MHz), the RTX 2000-10 (10 MHz), and the RTX 2001A-8 and -10 are available now in 84-pin PGA and PLCC packages. Military grades are also available.
COST: In 100-piece quantities: The 8-MHz RTX 2000 starts at $99, the 10-MHz version starts at $129, the 8-MHz RTX 2001A starts at $49, and the 10-MHz RTX 2001A starts at $76.
SECOND SOURCE: Zoran Corp (Santa Clara, CA).
CORE: Available in the Harris's advanced standard-cell and compiler library.

Description: The RTX 2000 is a high-performance 16-bit µP with on-chip timers, a interrupt controller, a multiplier, and two 256-word stacks. The manufacturer claims that the chip offers a sustained performance greater than 10 MIPS because each instruction requires only one clock cycle for execution. The chip's architecture lets designers add hardware accelerators and I/O devices that extend the chip's basic structure. The CMOS RTX 2000 operates between dc and the maximum clock rate. Power consumption is typically 5 mA/MHz.

Harris Semiconductor
Box 883
Melbourne, FL 32902
Phone (407) 724-3800
For more information, Circle No. 379

Status: Although Harris places its RTX 2000 in a RISC microcontroller category, the chip fits into the general-purpose µP category, too. The company expects that most of the chip's applications will fall into the real-time embedded-control realm. Because the chip directly executes Forth commands, Harris expects that designers will find doing real-time software development relatively easy. Harris designed the RTX 2000 using its advanced standard-cell and compiler library. Thus, designers can incorporate the device into ASICs.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram shows basic RTX 2000 architecture. The 2001A is a smaller version that lacks the hardware multiplier.
2. The ASIC-bus interface lets designers extend the chip's basic architecture with peripheral and I/O devices.

I—DATA-MANIPULATION INSTRUCTIONS Full set of math and logic instructions, which includes a single-cycle 16 × 16-bit multiplication operation as well as division and square-root operations. The architecture also allows 16- and 32-bit shifts. You can directly manipulate the top element of either the return or the parameter stack.
II—DATA-MOVEMENT INSTRUCTIONS
Access memory as bytes or words.
Memory-to-stack or stack-to-memory operations require two cycles.
Combine memory or I/O operations with ALU operations.
Access memory in LSB-MSB or MSB-LSB order.
"Streamed" memory access with automatic address update.
Access to 1M byte of memory space through page register.
III—PROGRAM-MANIPULATION INSTR
Intrapage calls require one cycle; interpage calls take three cycles. Return operations require either zero or one cycle.
Single-cycle conditional or unconditional branch operations. Conditional branches depend on the top-of-stack or on the index registers.
Single-level software interrupt.
IV—PROGRAM-STATUS-MANIP INSTR
Flags include interrupt enable, interrupt pending, carry, complex carry, byte order, and boot.
Automatic interrupt enable on return-from-interrupt operation.

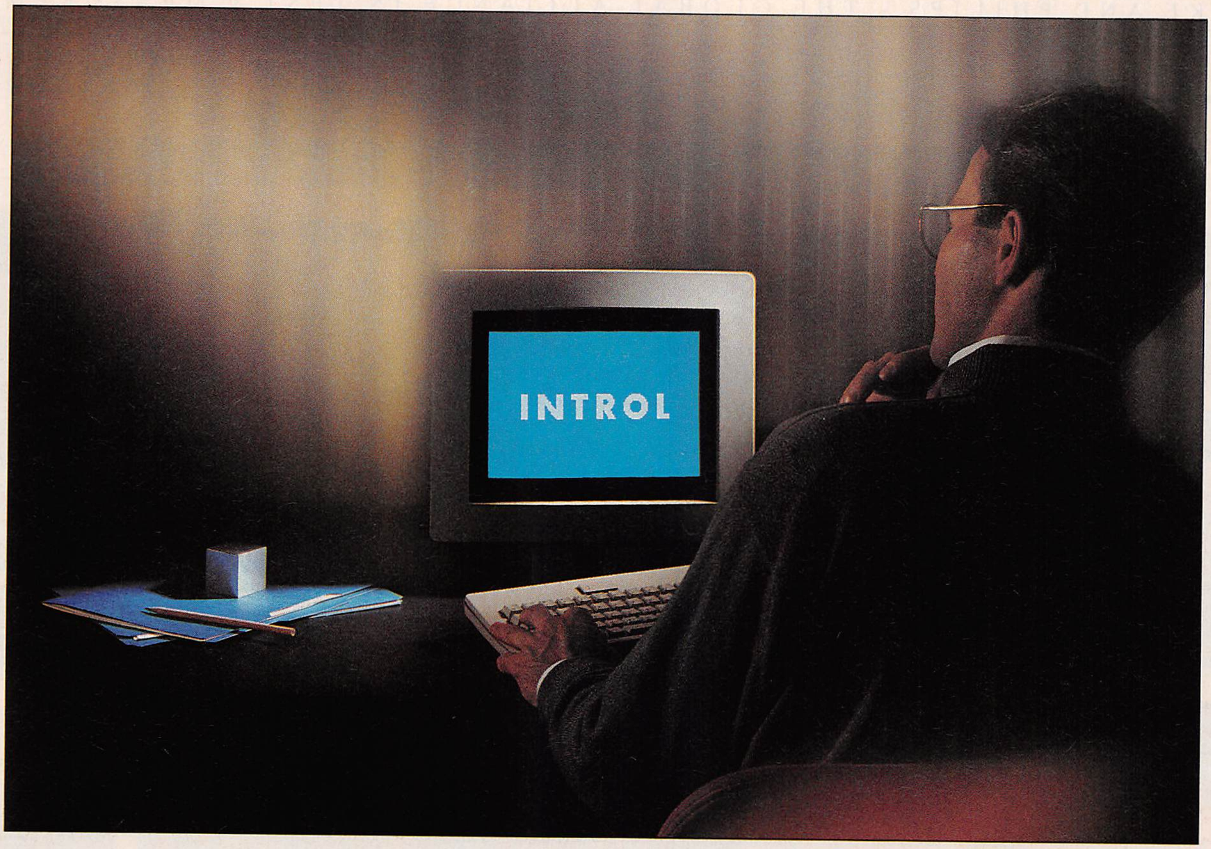
Specification summary: 16-bit CPU with 1M-byte address space. Bus cycles execute in 100 nsec with a 10-MHz clock. All instructions execute in 1 or 2 cycles, and the memory bus is active during every cycle. Additional I/O bus for high-speed transfer operations occurring simultaneously with memory-access and processing operations. The architecture includes two 64-word stacks, both of which may be active when memory- and I/O-transfer operations take place. Harris claims a peak data-transfer rate of 80M bytes/sec. On-chip peripheral devices include three counter/timer units and a 16-bit multiplier. The 107,000 mil^2 RTX 2000 and 80,000 mil^2 RTX 2001A are housed in an 84-pin PGA or an 84-pin PLCC package.

Software notes:
1. The RTX 2000 directly executes Forth statements; consequently, no assembly language exists for this processor.
2. Harris claims that the stack architecture is flexible enough to enable the chip to efficiently run many popular computer languages. The chip contains a parameter and a return stack.

HARDWARE — SUPPORT — SOFTWARE

From Harris: The Real-Time Express Development System (10 MHz, RTXDS-10; $2995) runs from within an IBM PC or compatible. Harris also offers 8- and 10-MHz development boards (from $1495) for those who want to write their own development software.
From others: The MicroProcessor Engineering (Southampton, UK; US agency is AMICS Enterprises, Rochester, NY) Power Board is a stand-alone unit that furnishes a variety of I/O ports and 500k bytes of RAM. VME Inc (Milpitas, CA) offers VMEbus development systems and stand-alone boards based on the RTX. Silicon Composers (Palo Alto, CA) also offers a variety of systems.

From Harris: Available software includes a target/host monitor; an IBM PC-based, C-development environment with interactive debugger; a Forth development system, which includes an RTX Forth cross-compiler; a disassembler; and a DOS file utility program. A Forth kernel and a multitasking operating system are also available.
From others: Laboratory Microsystems (Marina del Rey, CA), Forth Inc (Manhattan Beach, CA), and others have software packages for the RTX 2000 µP. MicroProcessor Engineering's Power Forth for its development board is an extended Forth-83 development environment.



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CIRCLE NO. 81

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FLUKE

CIRCLE NO. 87

TRANSPUTER FAMILY

16/32-BIT CMOS

AVAILABILITY: Now for 20-, 25-, and 30-MHz parts in PGAs, PLCCs, and PQFPs.
COST: In 100 qty PGAs: T222, $57; T400, $84; T425, $167; T800, $278; T801, $334.
SECOND SOURCE: None, but also manufactured at parent company SGS-Thomson's Carrollton, TX, fabrication plant.

Description: The Transputer family is a range of software-compatible 16-and 32-bit μPs. Each part has a CPU, on-chip SRAM (2k or 4k bits), timers, external memory interface, and 2 or 4 serial links. The links are 20M-bps DMA channels for communications and building multiprocessor systems. The serial links are DMA channels into the Transputer memory system and allow software processes to run on independent Transputers and communicate directly via the links. T8xx devices have an on-chip 64-bit FPU.

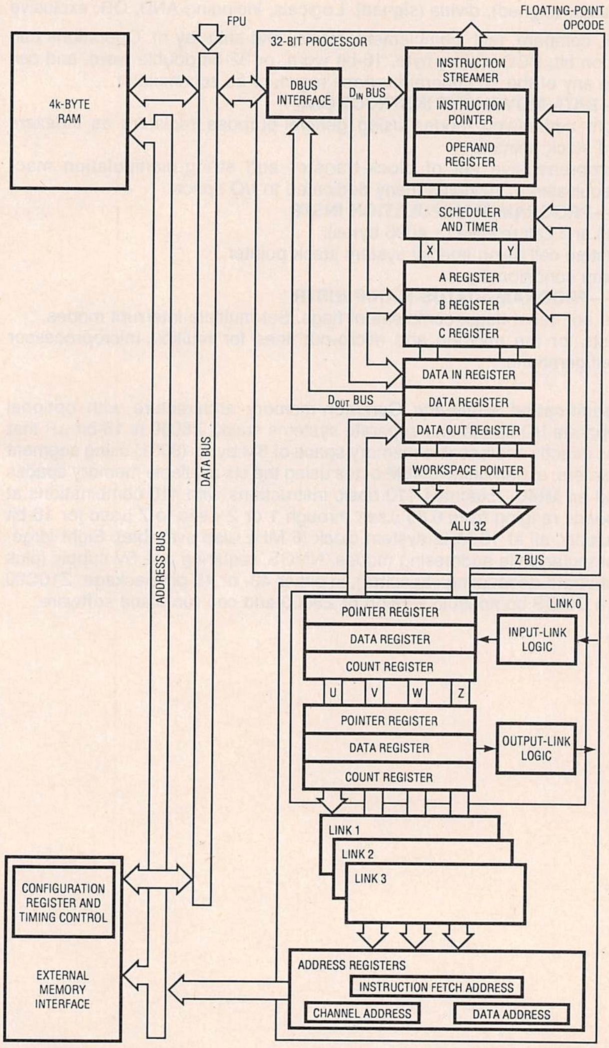
SGS-Inmos Limited
1000 Aztec West
Almondsbury
Bristol, UK
BS12 4SQ
Phone (0454) 616616
In US, phone (719) 630-4000
For more information, Circle No. 380

Status: Volume buildup has been slow. One possible explanation is that most of the applications have been for multiprocessor configurations (typically 4 to 10 Transputers), so designers have been engrossed by the challenge of developing practical parallelism. More than 1000 designs worldwide use the Transputer.

HARDWARE — CHARACTERISTICS — SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

Integer arithmetic, including multiply and divide. Logicals, shifts, and comparisons. T800 has on-chip IEEE floating-point add and subtract, multiply and divide, and square root, both 32 and 64 bits.



II—DATA-MOVEMENT INSTRUCTIONS

Memory-bandwidth block moves, 2-dimensional block moves for graphics bitblt. Load/store of local variables done relative to workspace pointer. Indexed load/stores available from address in A register. Immediate loads done 4 bits at a time. Large immediate values loadable from tables, instruction stream, or a sequence of special instructions.

III—PROGRAM-MANIPULATION INSTR

Conditional and unconditional jumps. Procedure call and return. Subroutine call and return. Computed jumps. Process (task) creation and deletion. 2-level priority and time-sliced scheduling with message passing and time events using built-in hardware. One level of interrupt.

IV—PROGRAM-STATUS-MANIP INSTR

Error flag detects overflow. Test, set, clear, stop-on-error instructions. One error flag per task priority level. Instructions for checking array bounds.

Specification summary: Family of 16- and 32-bit μPs designed for multiprocessing. Unique in that they have the hardware and software links that allow them to be hooked to each other for parallel processing. Four full-duplex, 20M-bps serial links driven by on-chip, 8-channel DMA provide basic multiprocessor communication links as well as I/O. One 5-MHz external clock generates 20-MHz chip clocks, giving 50-nsec instruction cycle. Submicrosecond interrupt latency, procedure call, and task switch. Most instructions take 1 or 2 cycles. Integer multiply takes 38 cycles; divide takes 39 cycles (less than 2 μsec). Single-precision floating-point add takes 7 cycles (350 nsec), floating-point multiply takes 11 to 18 cycles (550 to 900 nsec), and floating-point divide takes 16 to 28 cycles (800 to 1400 nsec).

Hardware notes:

1. Diagram is for T425. T800 is the same but adds an FPU. T801 is the same as the T800 except that the external memory interface is a nonmultiplexed data/address bus instead of the T800 multiplexed bus. T222 is the same as the T800 except that it has a 16-bit internal architecture and the FPU has been removed. The T400 is a low-cost variant with 2 links and 2k bits of on-chip memory.
2. Unlike most 32-bit machines, there is no group of general-purpose registers. Instead, substantial on-chip RAM plays equivalent role.
3. ALU fed from 3 accumulators forming a small 3-deep stack, allowing compact implied addressing.
4. The four serial links allow arrays of Transputers in multiprocessing with no bus saturation, which is the reason speed increase is said to be linear when more μPs are added.

Software notes:

1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack.
2. Two priority-ordered process queues are each supported by front and back registers, indicating a linked list of processes ready to run. Event-based multitasking is fully supported by a real-time kernel in microcode.
3. Supplier's Occam language said to facilitate programming multiple Transputer systems, but programmer must still study how best to partition task. Third parties have announced extensions to C to accomplish same ends.

HARDWARE — SUPPORT — SOFTWARE

Inmos offers development systems based on mother board for hosts such as the IBM PC, SUN, and DEC/VAX systems. Each mother board can accommodate Transputer Modules (TRAMs), which contain Transputer and memory. You can build multiprocessor systems by plugging multiple TRAMs into the mother board. Software controls the configuration. Third parties support the modules, which have industry standard pinouts. Memory sizes range from 32k to 8M bytes.

Inmos supplies compilers for hosts such as IBM PC, VAX (VMS), and Sun systems. ANSI C, Fortran, Pascal, and Occam are the languages that Inmos supports. Available software-debugging tools include network debugger, breakpoint, and trace facilities. Third-party vendors support Ada, Modula 2, and Prolog, and operating system environments such as Heios, Linda, and TransIdris.

Z8000/Z16C00

16/32-BIT NMOS AND CMOS

AVAILABILITY: Now for NMOS Z8000 at 6 and 10 MHz. Now for CMOS Z16C00 at 10 MHz; 16-MHz version will be available late in 1990.

COST: $4.72 (10k) for Z8000 in PLCC package.

SECOND SOURCE: SGS-Thomson, and Sharp for Z8000.

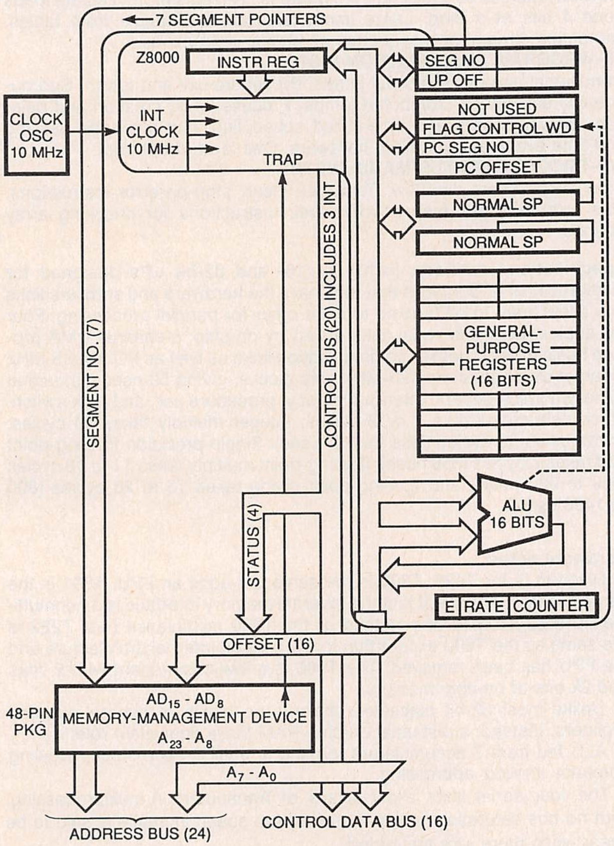
CORE: Zilog has both Z8000 and Z16C00 as cores in its in-house ASIC library and plans to use Zbus for its systems on silicon. The company says that 160×160-mil Z8000 core is small enough to leave room for other functions on practical 400×400-mil ASIC.

Description: One of the first µPs to have architectural features of a modern minicomputer. Original 16-bit Z8000 comes in 40-pin package for addressing 64k-byte memory or in 48-pin package for addressing 8M-byte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit µP, offering best CPU speed, interrupt handling, character-string search, and block moves.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000
For more information, Circle No. 381

Status: The Z8000 has found most acceptance in real-time control applications, particularly military, according to Zilog. The company has added the Z16C00 16-bit CMOS microcomputer to the family for real-time embedded control applications. The company is licensing its 16-bit core for customer applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
Supplier has companion peripherals suitable for both processors: For Z8000, a range of DMA, FIFO, data ciphering (NBS), communications, and counter/timer parts.
For Z16C00, a system general logic unit—16C20—contains memory support, DMA, interrupts, and I/O. For 16C01, a CMOS dual MMU80210 addresses 128 segments compatible with the 8010 NMOS MMU.

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed). Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n). Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulator.

II—DATA-MOVEMENT INSTRUCTIONS
Eight addressing modes using general-purpose registers as indexers and stack pointers.
Comprehensive set of block-transfer and string-manipulation macroequivalents, including many dedicated to I/O space.

III—PROGRAM-MANIPULATION INSTR
Call and call relative (±4096 bytes).
System call using special system stack pointer.
Jump conditionals.

IV—PROGRAM-STATUS-MANIP INSTR
Set and reset flags, complement flags. Set-multiple-interrupt modes.
Tests for the micro-in and micro-out lines for multiple-microprocessor configurations.

Specification summary: Common-memory architecture with optional separate I/O space and separate systems stack. Z8000 is 16-bit µP that has directly addressable memory space of 8M bytes (8001) using segment pointers, expandable to 48M bytes using the six available memory spaces and an MMU. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 µsec through 1 or 2 µsec to 7 µsec for 16-bit multiply, all at 10-MHz system clock (6 MHz also available). Eight large-computer-style addressing modes. NMOS, requiring one 5V supply (plus substrate-decoupling capacitor), in either 40- or 48-pin package. Z16C00 is a CMOS compatible version of Z8000 and can run same software.

HARDWARE — SUPPORT — SOFTWARE

From Zilog: Z16C00 development board ($250). 500-pg Z8000 technical manual.

From others: Tools available from Applied Micro, Boston Systems, Kontron, Orion, Single Board Solutions, and Tektronix. Contact supplier for addresses.

From Zilog: Real-time application software (IBM PC based). C compilers and cross assemblers. Contact supplier for names and addresses of software-support vendors.

Text continued on pg 161

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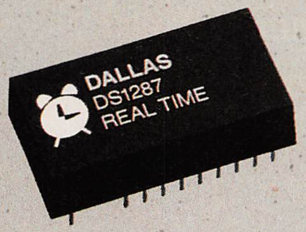

The DS1287 Real Time Clock retains data over 10 years in the absence of external power and is a direct replacement for the MC146818A.

And just to make sure you get every minute you've got coming, a freshness seal extends life by preventing lithium consumption until the equipment is first powered up.

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Recognizing that different designs need different approaches, we make clocks with four interfaces. If you didn't know you needed an interface until after the fact, try our phantom. The phantom interface fits into existing circuitry and is invoked with software; it appears and disappears on command. So it won't interfere with whatever else has to go on.

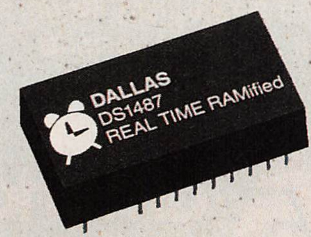
If you need the timer to mimic memory and sit on the memory bus, try our bytewide interface, which fits into a memory socket. If you need an interface for a PC/AT/OS2 or EISA, we have a PC interface. And, of course, we offer a serial interface.

Now Pick Your Options

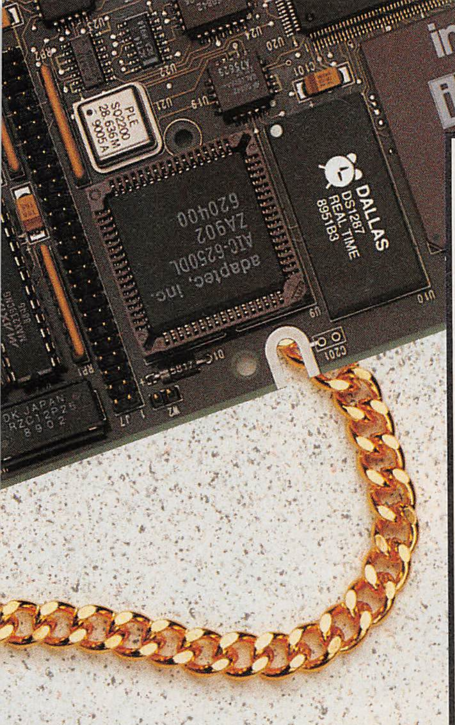
Have a look at our menu of selections.

Vital Memory
Many of our clocks provide what we call "vital memory," special nonvolatile RAM that stores information essential to the operation of the equipment.

Such as setup or configuration data to get the system going after a power failure. Or information that helps you keep track of computers and components. Like serial



The DS1487 RAMified Real Time Clock features 8K bytes of NV SRAM to store data essential to the operation of the equipment.



	Product Name and Number	Type of Interface	NV SRAM Bytes	Special Features
TIMEKEEPERS > 10 years of lithium +/- 1 minute/month. Quartz included. U.L. listed.	Real Time Clock DS1287	Multiplexed Bytewide Data/ Address Bus	50	Replaces MC 146818A; MS-DOS compatible; programmable interrupts; square wave output. Meets MCA and EISA NV RAM requirements.
	RAMified Real Time Clock DS1387, DS1397, DS1487		4K/8K	
	CPU Supervisory Stik DS2287		8K/32K	See above, plus power monitor and cold starts computer from keyboard.
	Watchdog Timekeeper DS1286	Conventional Bytewide SRAM Bus	50	CPU watchdog; programmable interrupts; square wave output; wake up interrupts.
	RAMified Timekeeper DS1386		32K	
	CPU Supervisory Stik DS2286		8K	See above, plus power monitor and cold starts computer from keyboard.
	SmartWatch/RAM DS1216 B, C, D	Conventional Bytewide SRAM and EPROM Bus with Phantom Interface	2K → 512K	Timekeeper built into a socket; mated SRAM converts to NV RAM.
	SmartWatch/ROM DS1216 E, F		(EPROM) 8K → 512K	
	NV SRAM with Phantom Clock DS1243Y, DS1244Y		8K/32K	NV SRAM packaged with timekeeper.
CHIPS Add lithium and quartz for time and NV SRAM.	Real Time Clock Chip DS1285	Multiplexed Bytewide Data/ Address Bus	50	Replaces MC 146818A; MS-DOS compatible; programmable interrupts; square wave output. Meets MCA and EISA NV RAM requirements.
	RAMified Real Time Clock Chip DS1385, DS1395, DS1491		4K/8K	
	Watchdog Timekeeper Chip DS1283, DS1284	Conventional Bytewide SRAM Bus	50	Programmable interrupts; square wave output. Controller provides battery backup circuitry for SRAM - 2.0 to 5.5 volt operation.
	Phantom Time Chip DS1215	Conventional Bytewide SRAM and EPROM Bus Controller with Phantom Interface	external	Battery backup circuitry for SRAM. Add-in real time clock uses same SRAM/EPROM signals.
	Serial Timekeeper Chip DS1202	3-Wire Serial Interface	24	2.0 to 5.5 volt operation; serial I/O for minimum pin count.

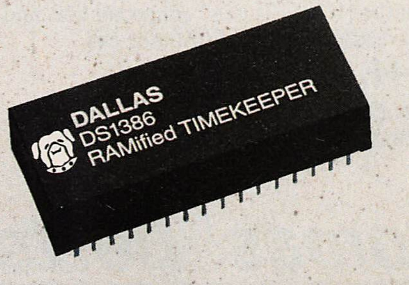
number, password, type of add-in boards, or field service warranty information.

You can choose the amount of vital memory you need — from 50 bytes to 32K bytes.

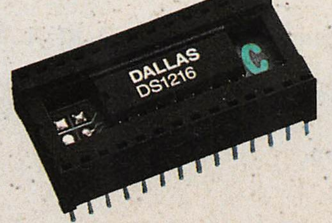
Watchdog Timer
Some clocks have watchdog timers that restart the system when the microprocessor is out of control. Your system can wake up or go to sleep thanks to programmable alarms. You can even set an alarm to go off on important dates — like January 1, 2000.

Easy Retrofit
Your systems are already designed and built? No problem. Some of our clocks retrofit to existing designs. They sneak in under an EPROM or a RAM — no changes to hardware required.

So if you need time, there isn't a better number to call.



The DS1386 RAMified Timekeeper guards against computer malfunction and mimics bytewide static RAM; it comes with 32K bytes of NV SRAM.



The DS1216 SmartWatch socket sandwiches between an EPROM and the printed circuit board and keeps perpetual time.

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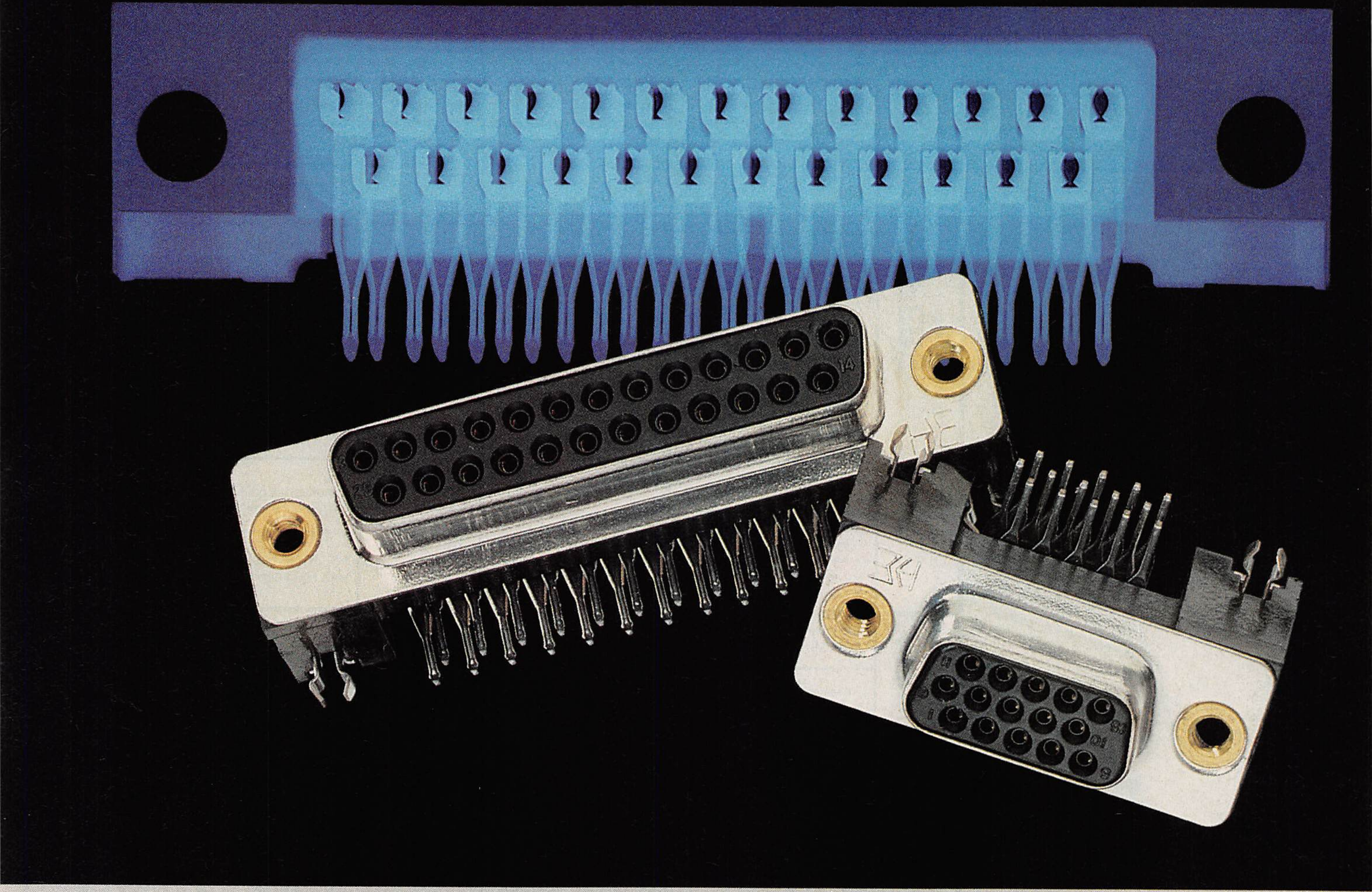
CIRCLE NO. 145

X-ray enlargement of 25 position HOLMBERG™ D-Subminiature connector



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1750A

16/32-BIT CMOS

AVAILABILITY: Now from Allied-Signal Microelectronics Center, LSI Logic, and United Technologies Microelectronics Center (UTMC).

COST: Allied-Signal charges \$760 (1000) for its part screened to 883C level B. The LSI Logic part costs \$1334 (100) screened to 883C in a PGA; a Class S part in a PGA costs \$4406 (100). The 883C part from UTMC, screened fully to Standard Military drawings (SMD), costs \$659 (100) for 12-MHz and \$791 (100) for 16-MHz devices. For high-reliability and military-temperature screening only, the price is \$555 (10 qty, 12 MHz) and \$666 (10 qty, 16 MHz).

SECOND SOURCE: In negotiation.

Description: MIL-STD-1750A defines instruction-set architecture for airborne computers. The standard leaves implementation to discretion of chip vendors. Allows use and reuse of available software support. Radiation-hardened and 883C level-S versions of many 1750A implementations available.

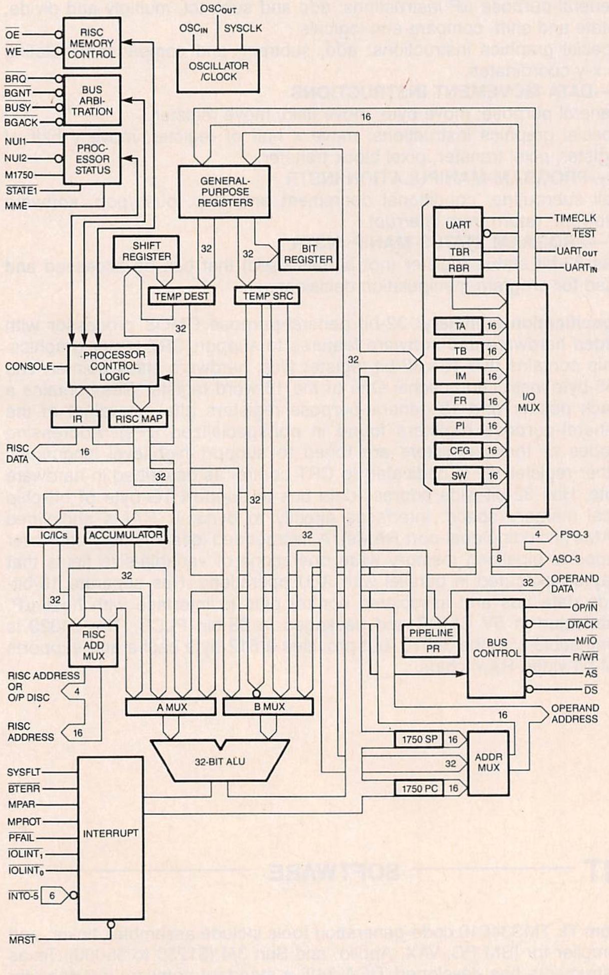
Status: Allied-Signal 40-MHz device has been in production for 3 years. A 50-MHz version will extend performance to 6.0 MIPS on the integer DAIS (Digital Avionics Instruction Set) mix and to 4.1 MIPS on full DAIS with floating-point unit. Allied-Signal MMU chip and LSI Logic's 1750A processor also in production. UTMC's unit is in full production as an 883C product that conforms to the Defense Electronics Supply Center standard military drawing. UTMC offers the device to 10^5 rad (Si) total-dose radiation hardness to meet data-sheet specifications.

Allied-Signal Microelectronics Center
9140 Old Annapolis Rd
MD 108
Columbia, MD 21045
Phone (301) 964-4047
For more information, Circle No. 382

LSI Logic
1501 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 433-7557
FAX (408) 433-7447
For more information, Circle No. 383

United Technologies Microelectronics Center (UTMC)
1575 Garden of the Gods Rd
Colorado Springs, CO 80907
Phone (800) 645-8862
For more information, Circle No. 384

HARDWARE CHARACTERISTICS SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, divide, and compare. Logicals and shifts. The instructions also provide bit-manipulation capabilities such as set, reset, and test. Single- and double-precision fixed floating-point and extended floating-point formats.

II—DATA-MOVEMENT INSTRUCTIONS
Instructions let you move data from register to memory, memory to register, between registers, and to the stack. Loads and stores in all formats plus test and set-bit operations.

III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional jumps and branches. Calls are also supported. Stack management instructions suitable for high-level languages. Handles 16 levels of prioritized interrupts.

IV—PROGRAM-STATUS-MANIP INSTR
Emulation-mode status register accessible through I/O instructions. Instructions for accessing status, interrupt-mask, and fault registers.

Specification summary: The Allied-Signal version is a single-chip implementation that includes timers, counters, a hardware multiply, and a floating-point unit. The LSI Logic L64500 1750A implementation has a 16-bit CPU, expandable to 32 bits depending on the operation. The L64550 includes MMU with memory expansion to 1M words, block-protect unit, memory-fault status register, bus-arbitration unit with 6 bus masters, start-up ROM interface, I/O port, trigger-go counter, and other options. Marconi's MAS281 is a radiation-hardened 3-chip silicon-on-sapphire (SOS) module. The MAS31750 is a single-chip SOS version.

Hardware notes:
Diagram is for the UTMC 1750AR. Functions as a stand-alone RISC processor providing 8 MIPS at 16 MHz. In the 1750A operation mode, a throughput of 750k IPS at 16 MHz is achieved using the DAIS mix. Basic µP accepts 64k bytes of memory, expandable to 1M byte using an MMU.

Representative 1750A microprocessors

Part number	Vendor	Technology	Price 883C	Price class S
BX1750A	Allied Signal Microelectronics	CMOS	\$750 (100)	—
L64500	LSI Logic	CMOS	\$1334 (1000)	\$4406 (1000)
MAS281	Marconi	CMOS/SOS	\$1600 (100)	\$8000 (20)
MAS31750	Marconi	CMOS/SOS	\$2000 (100)	\$10,000 (20)
1750AR	United Technologies Microelectronics	CMOS	\$659 (100)	\$1976–\$3950 (100)

HARDWARE SUPPORT SOFTWARE

You can use an IBM PC with the software tools to provide interactive simulation and debugging of system configurations.

Allied-Signal Microelectronics Center offers a development system for the A-S BX1750A that converts an IBM PC into a real-time, mappable monitor/debugger. An Ada source-level interface is under development. Tasco (Bellevue, WA) has an ICE pod for the HP 64000 development system. Call LSI Logic for contact phone numbers.

Assemblers and compilers are available from several outside sources. Mikros Systems offers high-level debug software for its single-board computer/IBM PC system.

UTMC offers a software package to aid in the development and debugging of system software and hardware. The software tool kit consists of a RISC or 1750 monitor, along with an interactive RISC simulator.

340X0 GRAPHICS μP FAMILY

32-BIT CMOS

AVAILABILITY: Now for 34010 and 34020. The 34082 floating-point unit is sampling now and is scheduled to be available in volume in the first quarter of 1991.

COST: The 34010 costs $23 (10k), the 34020 costs $89 (10k), and the 34082 floating-point unit costs $175 for samples.

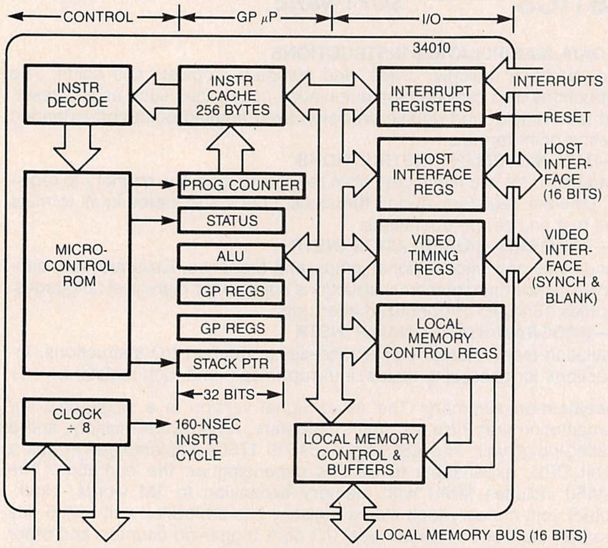
SECOND SOURCE: Under active consideration.

Description: This 32-bit CMOS μP family is optimized for graphics-display systems. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular μP instructions, it has specialized instructions for pixel manipulation. 1G-byte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits). The 34010 has a multiplexed, external 16-bit address/data bus; the 34020 is a full 32-bit machine. The 34020 is upwardly object-code compatible with the 34010 and features additional graphics-specific instructions.

Texas Instruments Inc
MOS Microcomputers
Box 1443, MS736
Houston, TX 77001
Phone (713) 274-2340
For more information, Circle No. 385

Status: Despite this μP family's specialized slant toward CRT graphics, it does have a general-purpose Von Neumann architecture and instruction set. Also, some of its attributes can be equally applied to other, nongraphics applications. In particular, the μP can do rapid bit manipulation of a large local address field. A number of IBM PC-based board-level products incorporate this part. X-Window terminals are an example of an application in which this family's graphics and general-purpose capabilities are utilized. One nongraphic area users are exploring is industrial control. In this area, the 340X0's bit manipulation and low cost relative to other 32-bit μPs are attractive, according to TI (even for consumer-oriented uses such as arcade games).

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Diagram represents 34010.
2. Added graphics features are embodied in the second 16 × 32-bit register file and among 28 16-bit I/O control registers. They allow programmable pixel and pixel-array processing for both monochrome and color systems of variable pixel sizes. Hardware incorporates 2-operand raster operations with Boolean and arithmetic operations, x-y addressing, window clipping, window pick operations, 1- to n-bit/pixel transforms, transparency, and plane masking.

I—DATA-MANIPULATION INSTRUCTIONS
General-purpose μP instructions: add and subtract, multiply and divide, rotate and shift, compare and logicals.
Special graphics instructions: add, subtract, and comparisons relating to x-y coordinates.
II—DATA-MOVEMENT INSTRUCTIONS
General purpose: move byte, move field, move register.
Special graphics instructions: move x half of register, move y half of register, pixel transfer, pixel block transfer.
III—PROGRAM-MANIPULATION INSTR
Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt.
IV—PROGRAM STATUS-MANIP INSTR
Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions.

Specification summary: 32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16 × 32-bit register files, hardware stack pointer, and 256-byte instruction cache. One of the 16-word register files contains a stack pointer and 15 general-purpose registers (the equivalent of the general-purpose registers found in nonspecialized μPs). Addressing modes of these registers are tuned to support high-level languages. Other register file is dedicated to CRT control as described in hardware note. Has 32-bit-wide address-data bus to support 1G byte of off-chip local memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A microcoded local-memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host μP. Fabricated in 5V CMOS and packaged in 68-pin PLCC. The 34020 is compatible with the 34010, but provides a 512-byte cache and supports 1M-bit video-RAM chips.

HARDWARE — SUPPORT — SOFTWARE

From TI: TMS34010 software development board ($1495), which plugs into IBM PC or compatible. Used for evaluation, familiarization, and software development, and comes with user interface and debugger software. TMS34010 XDS/22 emulator box ($14,995) operates as a standalone unit with nonintelligent terminal or with IBM PC or compatible as host. The TMS34020 software development board and hardware emulator system provide the same development functions for the 34020.
From others: Board-level and other hardware support now available from numerous sources. See TI's *TMS 34010 3rd-Party Guide* (call (800) 232-3200, ext 701, and ask for literature No. SPVB066C).

From TI: TMS34010 code-generation tools include assembler, linker, and compiler for IBM PC, VAX, Apollo, and Sun 3/4 ($1250 to $5000). Texas Instruments has developed TIGA-340, a standard software interface for the TMS340 family of graphics processors. Development tools for TIGA (Texas Instruments Graphics Architecture) include a $340 driver developer's kit, which helps software developers make existing software run on TIGA-compatible 34010 boards; a $1500 software developer's kit for those who want to develop direct 34010 code or custom downloadable extensions to TIGA, includes a 34010 C compiler, an assembler, bit-map font and math/graphics source-code libraries; and a $15,000 software-porting kit for hardware developers to make 34010-based systems TIGA compatible.
From others: See the TI TMS 34010 3rd-Party Guide.

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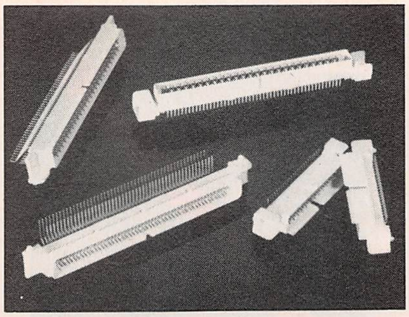

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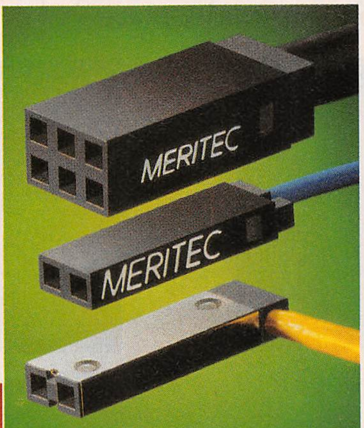

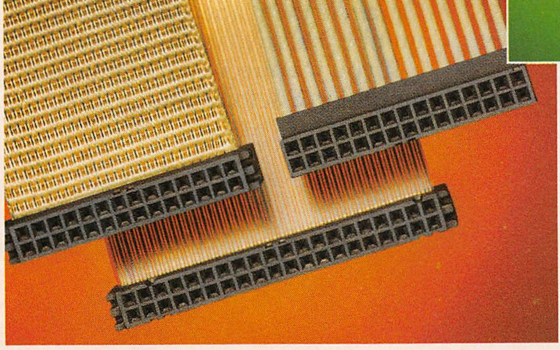

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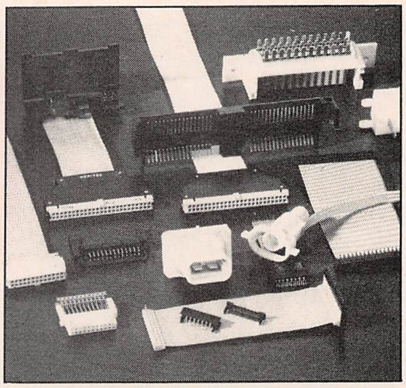

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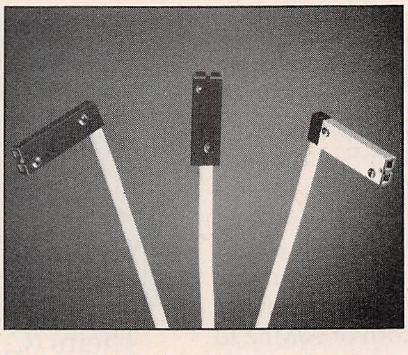

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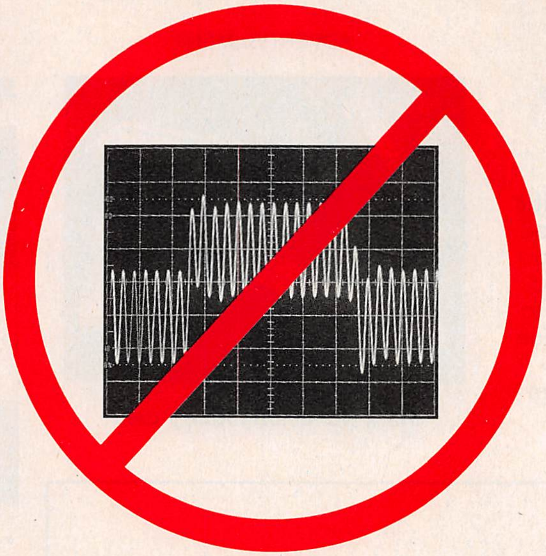

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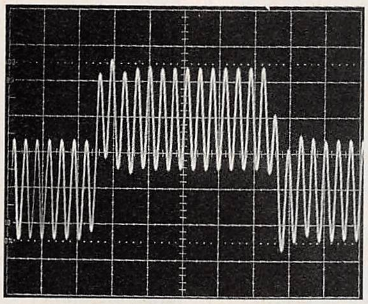
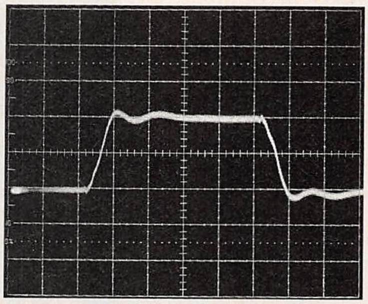


Theirs (C_L = 100pF)



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CIRCLE NO. 113

68000 FAMILY

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

AVAILABILITY: Now for 68000 to 12 MHz, 68HC000 to 16 MHz, 68HC001 to 16 MHz, 68020 to 33 MHz, 68030 to 50 MHz, and 68040 at 25 MHz.
COST: For lower-frequency devices in 1000 qty, prices range from $5.50 for 68000 and $7.10 for 68HC00X to $47 for 68020 and $95 for 68030. Sample qty pricing for 68040 is $795.
SECOND SOURCE: Hitachi, SGS-Thomson, and Signetics/Philips all licensed with mask interchange for 16-bit parts. No second sources for 68020, 68030, or 68040.
CORE: Motorola is using core with a mix of peripheral functions and glue logic in its 68300 family for embedded control. Signetics/Philips has the 68000 core in its ASIC library.

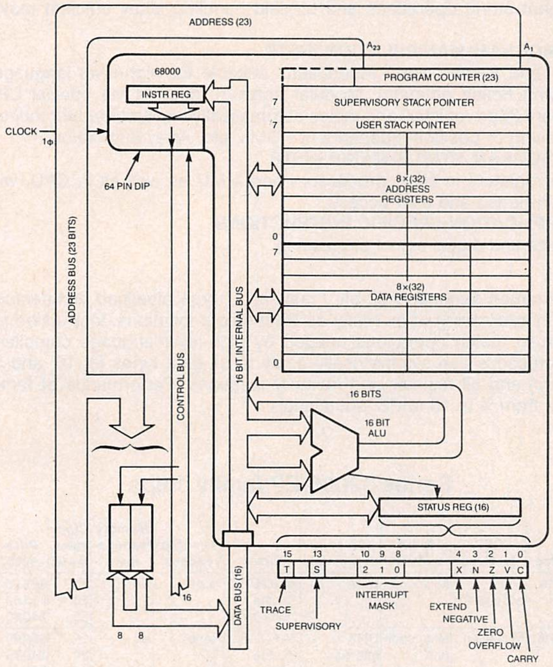
Description: 68000 architecture combines flexible 32-bit register set and large linear address space with powerful instruction set and flexible addressing modes. The 68040 is a full 68000-compatible µP containing an integer unit, floating-point unit (FPU), MMU, and instruction and data caches. The 680x0 family will get a boost from its 68300 derivatives in embedded control. 68300 family based on 68000 core and is software compatible.

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 891-2000
For more information, Circle No. 386

Status: The success of the 68000 family is largely due to the Apple Macintosh II and the family's popularity in Unix-based workstations. The H8/532 is the other microprocessor in the legal battle that involves Motorola's 68030.

CHARACTERISTICS

HARDWARE



Hardware notes:
1. Diagram of basic 16-bit 68000. Family offers growth path from 8-to 16- to 32-bit µPs. Performance results from multiple ALUs, 32-bit internal operation, and nonmultiplexed address and data buses.
2. Bottom-of-the-line 68008 has only 8-bit data bus and 20- or 22-bit address bus. 68010 is similar to 68000 but supports virtual memory. 68010 has 24-bit address bus. 68020 and 68030 are 32 bits throughout, including ALU and address and data paths. Both have instruction caches, and the 68030 also has a data cache and MMU. The 68040 adds an IEEE 754-compatible FPU.
3. Signetics/Philips 68070 includes 68000 CPU, two DMA channels, counter/timers, and an IC bus interface.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply and divide (signed and unsigned).
Logicals, rotates, and shifts.
Can handle bits, BCD nibbles, bytes, short (16 bits) and long (32 bits) words.
Floating-point coprocessors 68881/2 available.
II—DATA-MOVEMENT INSTRUCTIONS
Five basic address modes are register direct, register indirect, immediate, absolute, and program-counter relative. Postincrementing, predecrementing, offsetting, and indexing can be added to these models.
Can use eight 32-bit address registers as indexes or stack pointers. The eight 32-bit data registers can also serve as indexes.
III—PROGRAM-MANIPULATION INSTR
Branch and jump to subroutine. Branch conditionally.
Link and unlink instructions invoking one address register as frame pointer (used to establish temporary local environments in structured programming).
Seven levels of priority interrupts, including nonmaskable, with 256 possible interrupt vectors.
IV—PROGRAM-STATUS-MANIP INSTR
16-bit status register is software accessible.
Sophisticated trap operations help user debug programs.
Trace mode.
V—SYSTEM-CONTROL INSTRUCTIONS
Privileged instructions for operating systems and multiprocessor communication.

Specification summary: 68040 is the newest and highest-performance 68000 family member. This device is a 32-bit CMOS virtual-memory µP with multiple concurrent execution units. You can access the 4-way set-associative 4k-byte instruction and data caches simultaneously. The caches are organized in 64 sets of four 16-byte lines. The autonomous nature of the caches allows instruction-stream fetches, data-stream access, and third external access to occur during instruction execution. The 68040's parallelism allows multiple instructions that don't require external accesses to execute concurrently while the processor executes an external access for a previous instruction. The 68040 provides multimaster and multiprocessor support. Additionally, the processor can snoop the external bus during accesses by other bus masters to maintain coherency between the 68040 caches and external memory systems.
HDS-300 hardware/software development station ($15,000 to $20,000) provides real-time emulation of 68000-family µPs with bus-state-analyzer support and source-level debugging. MEX68KECB educational computer board is based on 68000. VM04 is a 68020-based 32-bit Versamodule interconnected within a target system using the 32-bit, asynchronous, Versabus interconnect standard. VME130 is a 68020-based, 32-bit VMEbus module using Eurocard mechanical format.

SUPPORT

HARDWARE

From third parties: Family widely supported by makers of universal µP development systems. Also, VMEbus system architecture is used in a range of applications with more than 150 independent suppliers of compatible products.
VersaDOS real-time operating system, system V/68 OS, CP/M-68K OS, concurrent DOS-68K OS, and VRTX real-time OS ($6775 from Hunter Systems). Unix support from Motorola includes direct ports of Unix System V. X assembler for Exormax and VME/10, X-C compiler VME/10, and Exormax for VAX/780 available.

SOFTWARE

From third parties: Supplier has catalog listing outside support for family. New type of support software lets 68000 run MS-DOS (8086) programs using emulation from Phoenix (Norwood, MA) and Insignia (London, UK; offices in San Francisco) or by using binary translation from Hunter Systems (Palo Alto, CA).

SERIES 32000

8/32-BIT, 16/32-BIT, 32/32-BIT NMOS AND CMOS

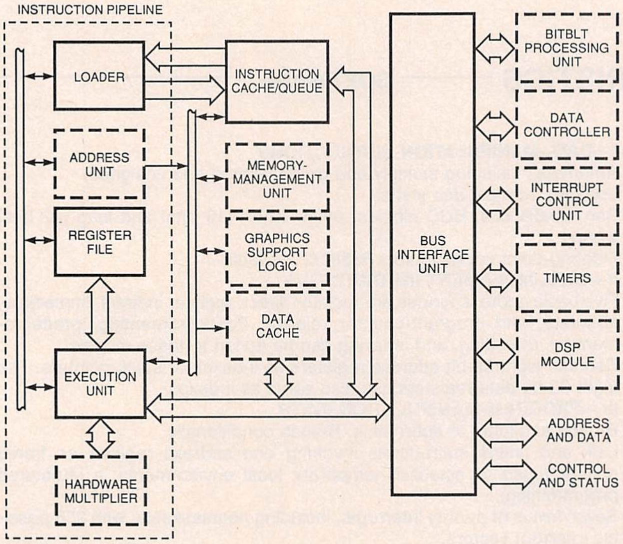
AVAILABILITY: Now.
COST: $11.50 to $600 (1000) (see table).
SECOND SOURCE: None.
CORE: National Semiconductor is using the 32000 as the basis for its application-specific embedded processors.

Description: A 32-bit µP family in which various models feature different-sized address and data buses. The 32-bit core processor is highly symmetric; that is, its instructions and addressing apply regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It also has reputation for needing less memory space for programs. Some models offer instructions to support graphics and DSP. A slave processor interface lets you expand the CPU's capabilities.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000
For more information, Circle No. 387

Status: The vendor recently introduced three family members: the NS32GX320, NS32FX16, and NS32CG160. Hardware and software integration techniques suit these processors for embedded applications such as page printers, facsimile machines, and multifunction office peripherals.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Dashed lines in diagram indicate optional modules for the 32000 family.
2. Floating-point chips (32081, 32181, and 32381) are examples of slave-type processors that vendor uses to extend CPU. These processors will be integrated on CPU when VLSI processing technology permits; they are transparent to programmer and recognize op codes not used by CPU.
3. Also available is the NS32580 that interfaces the CPU to the Weitek WTL3164 floating-point data path.

I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals, and bit manipulation throughout memory space and CPU registers.
II—DATA-MOVEMENT INSTRUCTIONS
Intelligent string operations and bit-field handling allow efficient movements.
III—PROGRAM-MANIPULATION INSTR
Stack- and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions.
IV—PROGRAM-STATUS-MANIP INSTR
Status registers in slave processors and MMU as well as in CPU, with both privileged and user access.
V—APPLICATION-SPECIFIC INSTRUCTIONS
Graphics and digital signal processing.

Specification summary: 32-bit, "maxi-mini"-type pipelined architecture. Uniform addressing of as many as 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, and 32 bits, etc) and all register and memory locations. Performance of family ranges from ¾ to 10 MIPS (sustained).

Series 32000/EP family chips

Device	DSP features	Bitblt support	On-chip peripherals	Buses	On-chip caches	Memory manage-ment	Clock rates (MHz)	Price (1000)
32FX16	DSP accelerator	Microcode	DMA	24 ADDRs 16 data multiplexed	None	No	15 20 25	$23.20 $33.60 $40.80
32CG160	Multiplier	Microcode and hardware	DMA interrupt timers	24 ADDRs 16 data multiplexed	None	No	15 20 25	$38.90 $40.70 $48.40
32GX320	Multiplier DSP instr	None	DMA interrupt timers	32 ADDRs 32 data	Instruction and data	No	20 25 30	$135.70 $155.25 $224.25
32GX32	None	None	None	32 ADDRs 32 data	Instruction and data	No	20 25 30	$105.80 $120.90 $197.20
32CG16	None	Microcode	None	24 ADDRs 16 data multiplexed	None	No	10 15	$11.50 $21.70
32532	None	None	None	32 ADDRs 32 data	Instruction and data	Yes	20 25 30	$465.00 $535.00 $600.00

HARDWARE — SUPPORT — SOFTWARE

From National: SYS32/20 converts IBM PC/AT into a Series 32000/EP development tool (from $3500). Development/evaluation boards are also available for each of the processors.
From others: ISE support for all the Series 32000/EP processors is available from Hewlett-Packard. Various vendors also offer turn-key solutions and/or design support for National Semiconductor's processors. Contact Series 32000/EP Marketing for details.

From National: GNX (Genix Native and Cross) development-tools software includes assembler package and choice of C, Pascal, or Fortran compilers available for native (Sys32/50) and cross-development environments. Software that enables the 32FX16 and 32GX320 to operate as either a FAX modem or data modem is also available.
From others: Various Postscript and Postscript-compatible language interpreters, as well as related software support (fonts, PCL, etc) are available for laser-printer-controller designs. DOS-based development tools are available from Introl.

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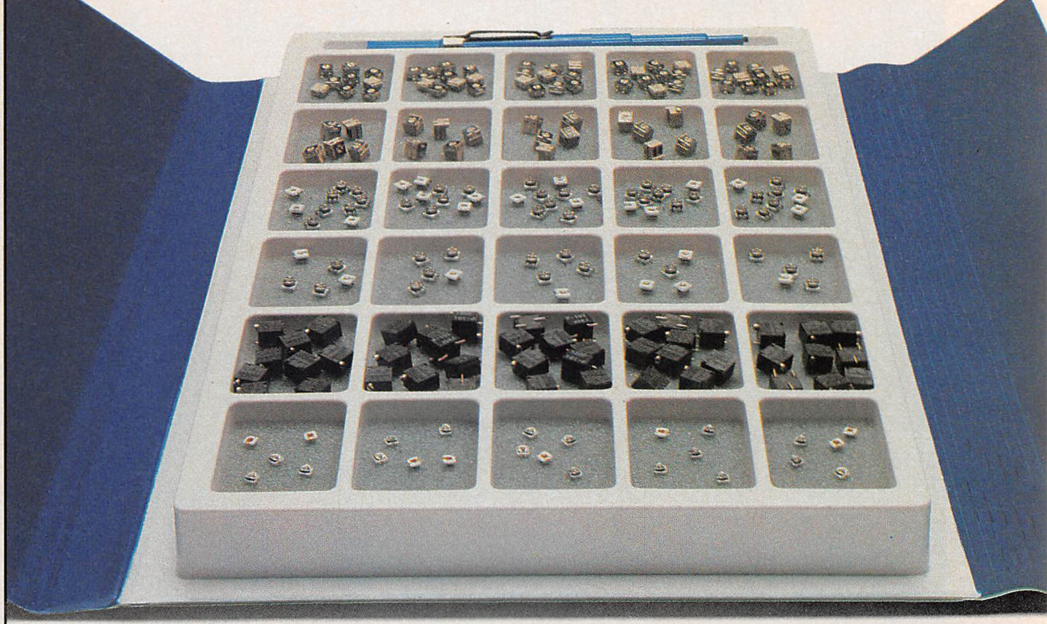

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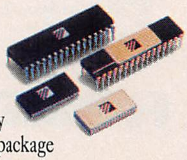

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VL 86C0X0 ARM

32-BIT CMOS

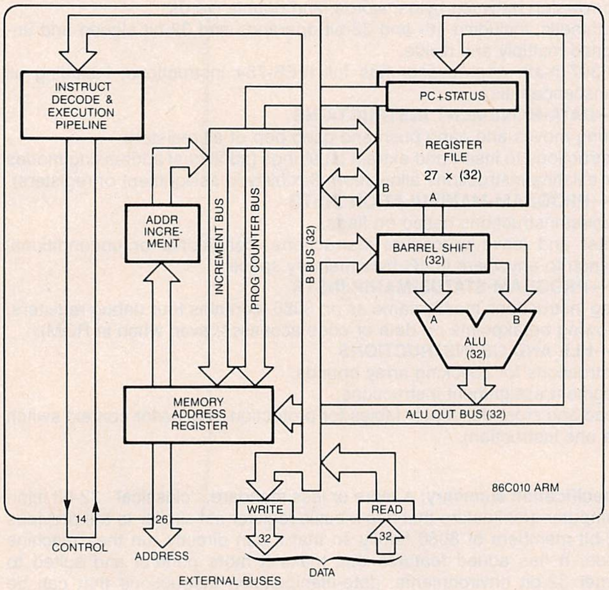
AVAILABILITY: Now for 86C010 and 86C020. VL86C050 I/O processor samples available now.
COST: \$39 (100) for 86C010; \$125 (100) for 86C020. 86C050 samples in PQFP \$80.
SECOND SOURCE: Sanyo Semiconductor Ltd sources the 86C010.
CORE: Part of VLSI's cell library. (Was designed by customer Acorn Computers using VLSI's semicustom tools.)

Description: ARM stands for Acorn-RISC machine. The VL86C020 is software compatible with the -010. The second-generation chip includes a 4k-byte unified instruction and data cache on chip. The cache uses 64-way set-associative replacement with random replacement to provide a 93% hit rate. Current devices operate at 30 MHz with 35-MHz operation available by year end as the μP migrates into a 1.0-μm process technology. Low power consumption of 0.5W suggests the part for embedded-controller applications.

VLSI Technology Inc
8375 S River Pkwy
Tempe, AZ 85284
Phone (602) 752-8574
For more information, Circle No. 388

Status: The company supplies evaluation boards, assemblers, and C compilers directly. The architecture of the chip is targeted at the embedded-controller market and provides performance similar to most competing RISC processors at lower cost. VLSI's goal is to sell the VL86C020 for less than \$60 in high-volume production. The cost of the cache memory is included in the processor price. Cost is kept low because of small die size (approximately 280 mils square in a 1.0-μm process) and 160-pin plastic quad flatpack packaging. A dedicated coprocessor bus necessitates the high pin count. The 86C020 has found application in laser printers, network controllers, disk controllers, and graphics subsystems.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, logicals, and comparisons. Bit clear. Shifts (barrel shifter with ALU).
II—DATA-MOVEMENT INSTRUCTIONS
Most data movements are by register-to-register instructions with option for multiple-register addressing. Only load and store operations to memory (typical of RISC). The VL86C010 includes a semaphore operation to support multiprocessing applications.
III—PROGRAM-MANIPULATION INSTR
Skip-type decision instructions (though old-fashioned, this simple approach can give fastest response in some cases). Branch instruction has option where combined PC and status register are copied in R14 data register for quick, simple return.
IV—PROGRAM-STATUS-MANIP INSTR
Usual status bits are combined with PC and mode-control bits in a 32-bit-long register. This combination allows all three elements to be saved in one fell swoop.

Specification summary: 32-bit CMOS Von Neumann (common memory) μP with RISC-style architecture. Has simple ALU with associated barrel shifter and set of 32 registers on CPU μP chip, 16 of which are accessible to programmer. Has some features expected in a large-memory-space machine: instructions and controls to handle virtual memory and caching. 32-bit external data bus and 26-bit external address bus allow linear addressing for external 64M-byte memory space (can be addressed on 8-bit-byte or 32-bit-word basis). Only simple load and store instructions for external memory. 10- to 12-MHz, 2-phase clock gives 4- to 5-MIPS sustained performance with 10 to 12 MIPS max. Interrupt latency is 2.75 μsec max. No provisions for separate I/O addressing, so I/O must be memory mapped. Fabricated in 2-μm CMOS; chip is 230 mils on side. 0 to 70°C temperature range. Packaged in 88-pin JEDEC Type-B leadless ceramic chip carrier and plastic leadless chip carrier.

Hardware notes:
1. In addition to the 86C010 μP, VLSI has an associated set of chips for memory (86C110), video (86C310), and I/O (86V410). For floating-point math, VLSI suggests one of the commercially available coprocessors.
2. Note the 27 registers. This number is less than on some RISC machines, but the registers do overlap, as is common in RISC, to speed interrupt service (overlapping gives automatic saving of data). Thus, a programmer sees 16 registers at most, and of these, 15 are general purpose.
3. Some provisions for memory management, including cache and virtual memory through abort-signal, mode-control bits.

Software notes:
1. Only 44 instructions, in keeping with the literal RISC concept.
2. Simple RISC instructions are said to ease the task of writing efficient high-level-language compilers.
3. User and supervisory modes; supervisory mode entered by software interrupt.

HARDWARE — SUPPORT — SOFTWARE

VLSI says that much of the hardware support comes from Acorn, such as a PC-form-factor board (\$2500) for software development. (Note: VLSI will probably bias its support toward the ASIC approach, in which the ARM μP will be considered a core around which the customer will be encouraged to apply "application-specific" I/O, memory, etc. Thus, VLSI's ASIC design tools might be considered part of the hardware support.)

VLSI indicates that most of the software support comes from Acorn, such as an assembler for the ARM's instruction set, a Basic interpreter, and compilers for popular high-level languages (C and Fortran-77). Compilers for artificial-intelligence languages (Cambridge Lisp and Prolog) are also available. Typical pricing for software packages is \$500.

80386 — 32-BIT CMOS

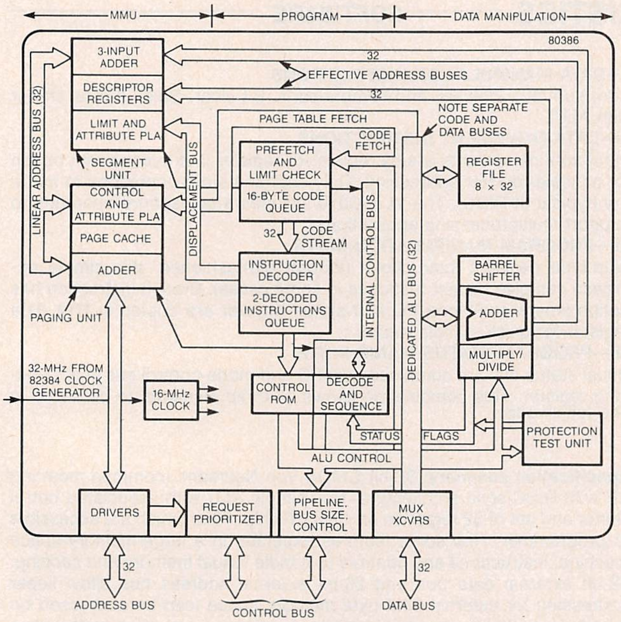
AVAILABILITY: 16-, 20-, 25-, and 33-MHz versions in production (at four locations). 80386SX, 80376 samples available now.
COST: In 1000 qty, $185 for 16-MHz 80386, $185 for 20-MHz 80386, $185 for 25-MHz 80386, $238 for 33-MHz 80386, $64 for 16-MHz 80386SX, and $112.50 for 20-MHz 80386SX. Low-power 16-MHz ($81) and 20-MHz 80386SX ($122.50) also available.
SECOND SOURCE: None.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 389

Description: The 32-bit 386 family of µPs is compatible with the 8086 and 80286 families. Included are address-translation registers and a 32-bit address bus for as many as 4G bytes of physical memory and 64T bytes of virtual memory (the SX and 376 processors have only a 24-bit address bus). Runs DOS, Windows, OS/2, Unix, iRMX, and iRMK. Virtual 8086 mode allows direct execution of 8086 software under new 32-bit operating systems. The 386SX permits the manufacture of less expensive systems with full 386 software capability.

Status: All indications point to the 80386 remaining the dominant 32-bit µP, certainly for the next five years. The 386 is the sole µP carrying the IBM PC momentum into the 32-bit world. Not satisfied that it owns the MS-DOS and OS/2 world, Intel is now aggressively after the Unix world and is in production with the 80376—a version of the 386 aimed at the embedded-controller world. Intel also offers the 80386SX, a version of the 386 that supplies a 16-bit data bus and a 24-bit address bus in standard and low-power versions.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. No on-chip cache, but 33-MHz 82385 cache controller ($82 (1k)) and 82395DX 16k-bit cache ($109 (1k)) can implement a cache.
2. On-chip MMU chip said to allow for memory management with no penalty in bus bandwidth (if off chip, supplier says, an extra cycle would be needed). Allows choices of segmentation or paging singly or in combination for multiuser protection and for virtual memory.
3. The 80386 has its own math coprocessor, the 80387, which costs $497 for 33 MHz, $406.85 for 25 MHz (1000).
4. Along with the 80387 and 82385, the 80386 can use the 82380 32-bit peripheral combination chip that incorporates DMA and interrupt support and interval timers, etc.
5. The 80376 is compatible with the 386 programming model, but cannot run 8086 or real-mode programs. The chip has a 16-bit external bus.

I—DATA-MANIPULATION INSTRUCTIONS
Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter).
Conversion between bytes, words, and double words.
Arithmetic, including 16- and 32-bit operands and 32-bit signed and unsigned multiply and divide.
(80387 math coprocessor has full IEEE-754 instructions, including all transcendentals.)
II—DATA-MOVEMENT INSTRUCTIONS
String moves and gang push and gang pop of all registers.
Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers).
III—PROGRAM-MANIPULATION INSTR
Repeat instructions based on flags.
Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4G-byte memory space.
IV—PROGRAM-STATUS-MANIP INSTR
Flag instructions mostly same as on 8086 (contains four debug registers, allowing breakpoints on data or code accesses, even when in ROM).
V—HLL AND OS INSTRUCTIONS
Instructions for checking array bounds.
Segment assignment instructions.
Load and store descriptor tables for protection (processor context switch via one instruction).

Specification summary: A more or less standard, "classical" 32-bit minicomputer architecture that has a basic register set similar to the previous 16-bit members of 8086 family so that it can directly run their machine code. It has added features that make it more general and suited to larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. Fabricated in 1.5-µm CMOS (supplier calls it CHMOS-III), the chip is expected to consume no more than 400 mA at 32-MHz external clock (16 MHz internal). Packaged in 132-lead ceramic PGA.

Software notes:
1. Only those instructions beyond basic 8086 instructions described.
2. 80386 said to be object-code compatible with previous members of 8086 family and can run their operating systems. There is a "virtual 8086" mode in which 8086 (and 8088) code can be run within the protected 386 environment.

HARDWARE — SUPPORT — SOFTWARE

ICE-38625D in-circuit emulator ($22,495) supports 386DX µP to 25 MHz; ICE38633D ($33,000) supports to 33 MHz. ICE386SX in-circuit emulator ($22,500) supports 386SX to 20 MHz. ICE376D in-circuit emulator ($18,495) supports 376 to 16 MHz. All Intel ICE in-circuit emulators for the 386 family operate on a common emulator base. They provide control and display software with a common Intel windowed user interface with drop-down menus and source-code display hosted on DOS on PC and PS/2 systems. The iPAT Performance Analysis Tool provides real- and protected-mode software analysis with high-level access to target-system performance analysis and test-case coverage in real time for target systems based on the 386 family at clock speeds to 20 MHz. An iPAT-386 probe supports the 386DX µP. You can also interface the iPAT-386 to the probes of ICE in-circuit emulators for the 386DX, SX, and 376 µPs. Various Multibus I and II single-board computers are also available from Intel and other vendors for the 386DX µP.

From Intel: ASM-386 macroassembler ($600), RLL-386 binder and system software builder utilities ($600), and the MON-386 serially hosted debug monitor ($995). The C-386, Fortran-386, and PL/M-386 compilers (each $900) support 386 µP family protected-mode software cross development on DOS hosts. VAX/VMS kit support including ASM, RLL, compilers of choice, and VMS DB-386 incorporating a 386 system software simulator is also available on MicroVAX ($14,000) and VAX ($18,000) systems for cross development.
From others: Rapidly growing third-party support. Most important are MS-DOS and forthcoming OS/2 from Microsoft (Bellevue, WA). (There are variations in DOS such as Concurrent DOS by Digital Research (Monterey, CA).) Unix V from AT&T (Morristown, NJ) and Zenix from Microsoft also available. Real-time executives offered by Ready Systems (Palo Alto, CA), JMI Software (Spring House, PA), and others. In addition, there are dual combinations of operating systems such as Unix-DOS, CTOS-DOS, and DOS-DOS.
Note: Some software depends on 386 mode.

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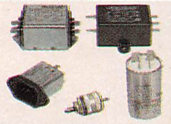
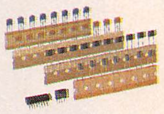

EMI/RFI Suppression Filters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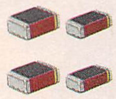
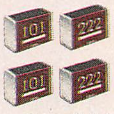
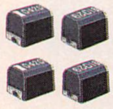
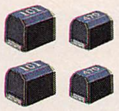
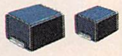
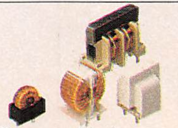

Ferrite Chip EMI Suppressors (Ferrite Chip Beads)

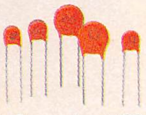

Micro Chip EMI Filters

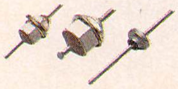

Leadless EMI Filters

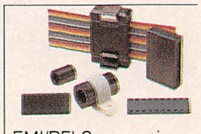

Power-Line Leadless Inductors

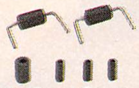

Leadless Line Choke SF Coils


Common Mode Choke Coils/Line Choke Coils (SF Type)

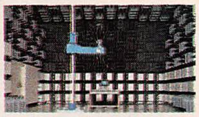

UL Recognized (CSA, VDE, SEV, SEMKO, BS) Ceramic Capacitors


Feed-Through Ceramic Capacitors


EMI/RFI Suppression Ferrites


Ferrite Bead Cores

Varistors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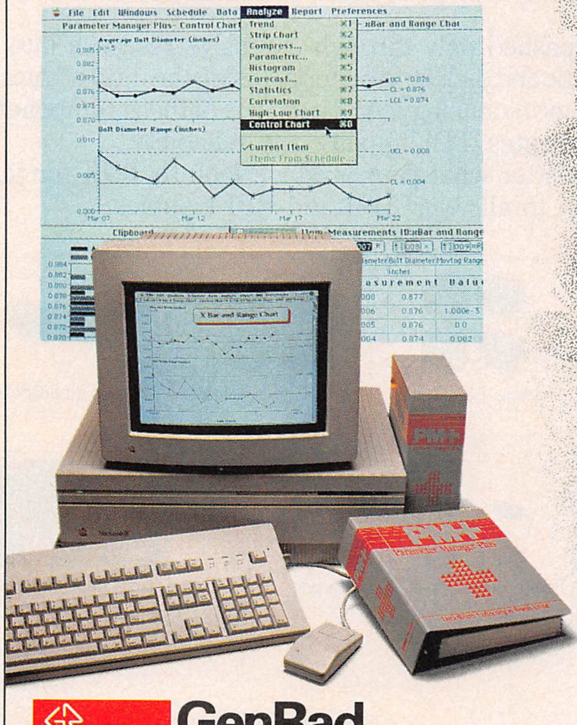

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CIRCLE NO. 77

80486

32-BIT CMOS

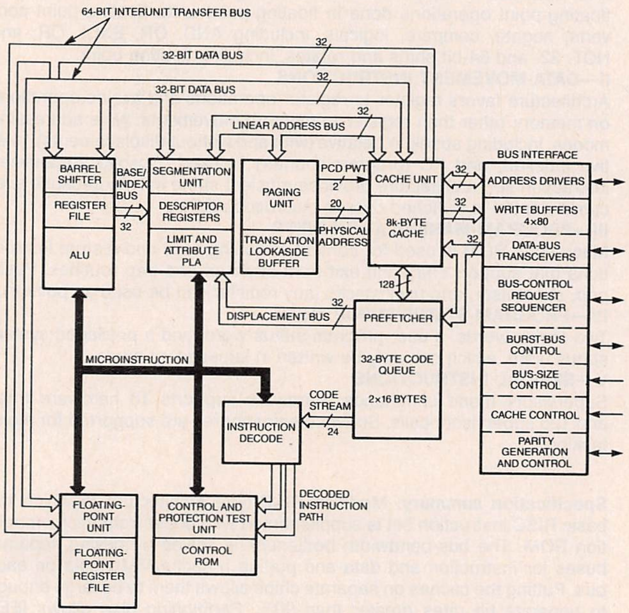
AVAILABILITY: 25- and 33-MHz versions now in production.
COST: In 1000 qty, $760 (25 MHz) and $1003 (33 MHz).
SECOND SOURCE: None.

Description: The i486 CPU comprises an enhanced 80386 CPU, an enhanced 80387 math coprocessor, an 82385 cache controller, an 8k-byte combined code and data cache, and a paging and memory-management unit. The i486 is binary compatible with 386/387 processor software but is 2 to 4× faster because of enhanced execution pipelining and higher integration. The i486 CPU adds several new instructions that support caches and multiprocessor operating systems. A byte-swap instruction allows the i486 CPU to read data in either big- or little-endian format. A burst bus allows the i486 to fill the on-chip cache with 16 bytes of data in five clock cycles.

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 390

Status: 25-MHz version has been in production since late last year; the 33-MHz version went into production in May of this year. Many servers and multiprocessing systems—in addition to the expected traditional desktop personal computers—are based on the i486 CPU. The company expects to increase performance by offering the chip at higher operating frequencies.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. 8k-byte unified instruction and data cache is located on chip. The cache lets the CPU read 16 bytes of code into the prefetch queue in one clock. A cache hit rate of better than 90%, for most applications, greatly reduces memory bus utilization for memory reads and improves system performance.
2. The Turbocache486 module ($299 for 64k-byte version and $399 for 128k-byte version at 33 MHz in 1000 qty; 25 MHz also available) is a complete second-level write-through cache controller and SRAM. The module contains the 82485 cache controller ($89 (25 MHz) and $99 (33 MHz) in 1000 qty). The module's look-aside design lets you add the module as an option much as the 387 was an option to 386 systems.
3. An on-chip MMU allows memory management identical to the 386DX CPU. The MMU allows segmentation, paging, or a combination of both for multiuser protection and for virtual memory.

I—DATA-MANIPULATION INSTRUCTIONS
Byte swap for converting between little- and big-endian data. Compare and exchange instruction. Exchange and add instruction. Floating-point instruction set from 387 math coprocessor added to i486 CPU.
II—DATA-MOVEMENT INSTRUCTIONS
Information not provided by manufacturer.
III—PROGRAM-MANIPULATION INSTR
Information not provided by manufacturer.
IV—PROGRAM-STATUS-MANIP INSTR
Information not provided by manufacturer.
V—HLL AND OS INSTRUCTIONS
Instructions for flushing and invalidating the caches.

Specification summary: A standard 32-bit architecture containing the same register set as its predecessor, the 386DX CPU. The 486 adds a small cache and floating-point processor as well as the instructions and control bits to support these features. The part is fabricated using a 1-μm process and consumes less than 700 mA at 25 MHz. The μP is packaged in a 168-pin ceramic PGA.

HARDWARE — SUPPORT — SOFTWARE

ICE48633D In-circuit emulator ($49,000) supports the 486 μP to 33 MHz with real-time execution control over prototype 486-based systems. ICD48625D in-circuit debugger ($9500) is a hardware-assisted real-time debug monitor supporting 486 μP to 25 MHz. ICD48625D supports execution breakpoints, including cached breaks, control of 486 μP execution, and access to registers and system memory. A standard logic-analyzer interface supports cross triggering between ICD486 and a high-speed logic analyzer. The ICD48625D in-circuit debugger is hosted on DOS PC and PS/2 systems. Host software uses the common Intel windowed interface model with drop-down menus and source-code display.

From Intel: Intel's i486 assembler, compilers, system utilities, and software debuggers are intended for computer-system software development requiring access to the full native-mode architecture models of the 486 μP. ASM macroassembler ($600); RLL binder and system-software-builder utilities ($600); and C, Fortran, and PL/M compilers (each $900) support 486-family protected-mode software cross development by generating 486 instructions in code developed on DOS hosts. Language kits ($4500) including ASM, RLL, a compiler of choice, and the DB debugger are also available. VAX/VMS kit support including ASM, RLL, and a compiler of choice is available on MicroVAX ($14,000) and VAX ($18,000) systems for cross development.

CLIPPER

32-BIT CMOS

AVAILABILITY: Now for 25- and 33-MHz C200 chip sets and modules, the 211 CPU/FPU, 40- and 50-MHz C300 chipsets and modules, and the C311 CPU/FPU. The 40-MHz C4 will sample late this year.
COST: All 1000 qty: At 33 MHz, the C211 CPU/FPU costs $69, the C200 chip set costs $229, and the C200 module costs $424. At 40 MHz, the C311 costs $160, the C300 chip set costs $336, and the module costs $536. At 50 MHz, the C311 costs $191, the C300 chip set costs $495, and the C300 module costs $695.
SECOND SOURCE: Samsung Semiconductor.

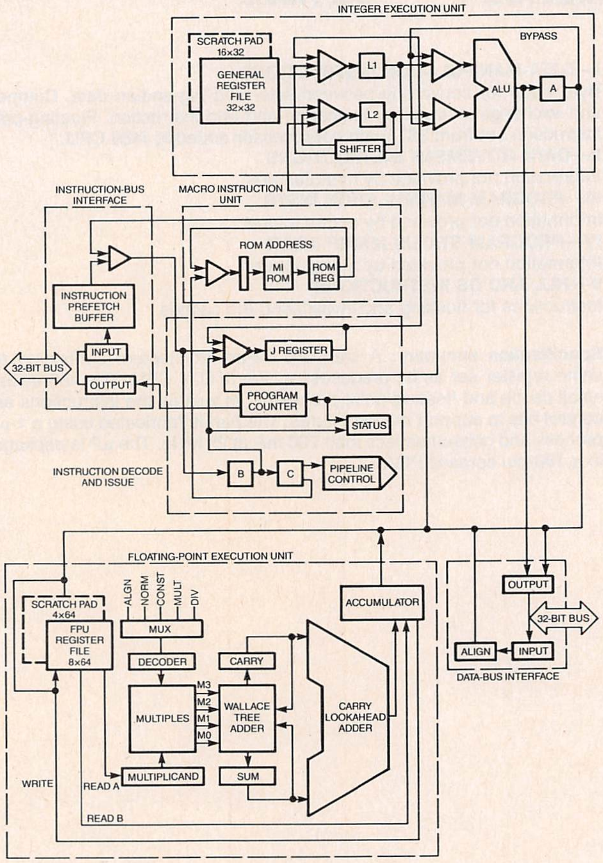
Description: CMOS RISC-based µP has a dual-bus Harvard architecture. 3-chip set includes a CPU that incorporates a floating-point unit (FPU) and two cache/MMU chips: one for instructions and one for data. Available in first- and second-generation versions in modules, chip sets, and individual chips. The upcoming C4 is a superscalar implementation.

Intergraph Corp
Advanced Processor Div
2400 Geng Rd
Palo Alto, CA 94303
Phone (415) 494-8800
For more information, Circle No. 391

Status: The company claims over 45,000 Clipper modules have been shipped through May 1990, giving Clipper a large, but narrow, installed base—Intergraph and DuPont account for more than 98% of sales.

CHARACTERISTICS

HARDWARE



Hardware notes:
1. The CPU chip has RISC-like ALU plus a CISC-like macroinstruction ROM and FPU. The other two chips are identical pin-programmable cache/MMU chips, so one can be used for instruction caching and the other for data caching. The instruction cache carries the CPU's instruction program counter. The 4096-byte capacity of each cache plus the sophisticated caching control (2-way set associative) gives the Clipper a hit ratio greater than 90%.
2. Each cache supports virtual memory via the on-chip MMU. The caches (especially the data cache) operate on a physical memory basis, so less flushing is needed. The C200 requires 135-nsec memory devices; the C300 requires 90-nsec memory devices.
3. CPU uses sophisticated pipelining with provision for bypassing.
4. C4 will be a 2-chip set (CPU and FPU) with a 64-bit instruction/data bus. C4 will be binary compatible with C300.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, divide (32-bit integer and 32- and 64-bit IEEE floating-point operations done in floating-point unit), floating-point converts, negate, compare, logicals, including AND, OR, EXCL OR, and NOT. 32- and 64-bit shifts and rotates, including floating point.
II—DATA-MOVEMENT INSTRUCTIONS
Architecture favors register-to-register operations and avoids operations on memory other than register-to-memory movements. Nine addressing modes, including absolute, relative (with and without displacements), relative indexed, and PC (program-counter) indexed. Despite streamlined instruction set, architecture provides efficient string moves because execution control is switched over to macrocode ROM.
III—PROGRAM-MANIPULATION INSTR
Macrocode ROM is used for context-switching save and restore instructions that support entry and exit from interrupt and trap routines. Push, pop, supervisor, and user stacks (any register can be used as pointer).
IV—PROGRAM-STATUS-MANIP INSTR
Two status words, a user-program status word, and a privileged system status word, which can only be written in supervisory mode.
V—SPECIAL INSTRUCTIONS
Supervisory mode commands. Hardware supports 18 hardware traps and 128 supervisory calls. Software semaphores are supported for multitasking.

Specification summary: Modified RISC-type architecture in which the basic RISC instruction set is supplemented with boost from microinstruction ROM. The bus-bandwidth bottleneck is solved by having separate buses for instruction and data and putting a cache/MMU chip on each bus. Putting the caches on separate chips allows them to be large enough to generate hit rates greater than 90%. Partitioning also allows IEEE 64-bit floating-point operations to be incorporated on CPU chip so there is no off-chip delay. There is no need for CPU to have separate multiply-divide hardware because these operations can be done in the FPU. The chips are sold mounted with clock on a 3.5×4.5-in. multilayer-pc card with 96-pin DIN connector. C200 chips are also available separately.

Software notes:
1. Clipper's 164 instructions are a balance between 1-cycle-RISC and multicycle-CISC commands. The RISC takes care of the simpler, most frequently used instructions. The CISC macrocode takes care of complex instructions such as floating/integer conversion, character-string manipulation, save and restore registers, and trap/interrupt entry and return sequences.
2. C200 and C300 instructions are compatible.

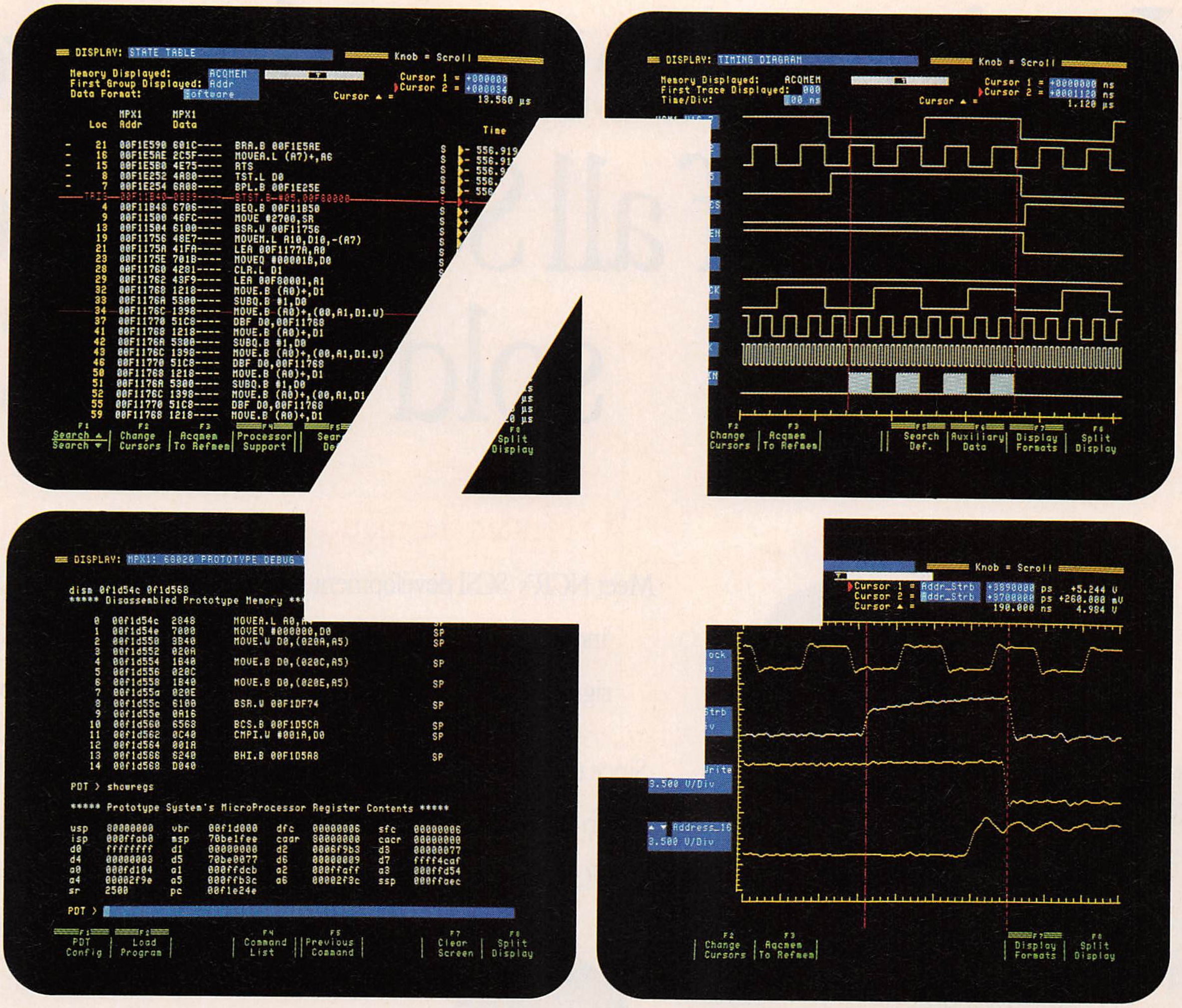
SUPPORT

HARDWARE

The Clipper Module card integrates the three Clipper chips into a functioning CPU. It provides the clock and program-counter wiring and a 96-pin DIN connector. User must provide the bus buffers externally. Intergraph supplies development systems that provide a 33-MHz Clipper CPU, 8M bytes of RAM, 156M bytes of hard-disk storage, and an Ethernet interface. Software includes Clix (which is based on Unix System V), a C compiler, a loader/debugger, and utilities.

SOFTWARE

A wide array of standards-based software is available from Intergraph, including Clix V.3.1 (based on Unix V.3.1) operating system; optimizing compilers for C, Fortran, and Pascal; RFS, NFS, and TCP/IP networking software; and X-windows windowing interface. More than 500 third-party packages are available, including compilers for Lisp, Ada, and other languages; tools and utilities; end-user application packages such as Word Perfect, Q-Calc, Q-Office+, Masterplan, and UniPlex II Plus; and the Ingres, Informix, and Oracle database programs.



```
DISPLAY: STATE TABLE                              Knob = Scroll
 Memory Displayed:       ACQMEM                    Cursor 1 = +000000
 First Group Displayed:  Addr                     ▸Cursor 2 = +000034
 Data Format:            Software         Cursor ▲ =           13.560 µs

        MPX1      MPX1
   Loc  Addr      Data                                          Time

 -  21  00F1E590  601C----  BRA.B 00F1E5AE                S ▸- 556.919
 -  16  00F1E5AE  2C5F----  MOVEA.L (A7)+,A6              S ▸- 556.91
 -  15  00F1E5B0  4E75----  RTS                           S ▸- 556.9
 -   8  00F1E252  4A80----  TST.L D0                      S ▸- 556.
 -   7  00F1E254  6A08----  BPL.B 00F1E25E                S ▸- 556
 ---TRIG--00F11B40--0839-----BTST.B-#05,00F80000--------- S ▸-
     4  00F11B48  6706----  BEQ.B 00F11B50                S ▸+
     9  00F11500  46FC----  MOVE #2700,SR                 S ▸+
    13  00F11504  6100----  BSR.W 00F11756                S ▸+
    19  00F11756  48E7----  MOVEM.L A10,D10,-(A7)         S
    21  00F1175A  41FA----  LEA 00F1177A,A0               S
    23  00F1175E  701B----  MOVEQ #00001B,D0              S
    28  00F11760  4281----  CLR.L D1                      S
    29  00F11762  43F9----  LEA 00F80001,A1
    32  00F11768  1218----  MOVE.B (A0)+,D1
    33  00F1176A  5300----  SUBQ.B #1,D0
    34  00F1176C  1398----  MOVE.B (A0)+,(00,A1,D1.W)
    37  00F11770  51C8----  DBF D0,00F11768
    41  00F11768  1218----  MOVE.B (A0)+,D1
    42  00F1176A  5300----  SUBQ.B #1,D0
    43  00F1176C  1398----  MOVE.B (A0)+,(00,A1,D1.W)
    46  00F11770  51C8----  DBF D0,00F11768
    50  00F11768  1218----  MOVE.B (A0)+,D1
    51  00F1176A  5300----  SUBQ.B #1,D0
    52  00F1176C  1398----  MOVE.B (A0)+,(00,A1,D1
    55  00F11770  51C8----  DBF D0,00F11768
    59  00F11768  1218----  MOVE.B (A0)+,D1
```

```
DISPLAY: TIMING DIAGRAM                           Knob = Scroll
 Memory Displayed:       ACQMEM                    Cursor 1 = +0000000 ns
 First Trace Displayed:  000                      ▸Cursor 2 = +0001120 ns
 Time/Div:               100 ns          Cursor ▲ =          1.120 µs
```

```
DISPLAY: MPX1: 68020 PROTOTYPE DEBUG

 dism 0f1d54c 0f1d568
 ***** Disassembled Prototype Memory ***

     0  00f1d54c  2848        MOVEA.L A0,A
     1  00f1d54e  7000        MOVEQ #000000,D0              SP
     2  00f1d550  3B40        MOVE.W D0,(020A,A5)           SP
     3  00f1d552  020A
     4  00f1d554  1B40        MOVE.B D0,(020C,A5)           SP
     5  00f1d556  020C
     6  00f1d558  1B40        MOVE.B D0,(020E,A5)           SP
     7  00f1d55a  020E
     8  00f1d55c  6100        BSR.W 00F1DF74                SP
     9  00f1d55e  0A16
    10  00f1d560  6568        BCS.B 00F1D5CA                SP
    11  00f1d562  0C40        CMPI.W #001A,D0               SP
    12  00f1d564  001A
    13  00f1d566  6240        BHI.B 00F1D5A8                SP
    14  00f1d568  D040

 PDT > showregs

 ***** Prototype System's MicroProcessor Register Contents *****

 usp   00000000   vbr   00f1d000   dfc   00000006   sfc   00000006
 isp   000ffab0   msp   70be1fee   caar  00000000   cacr  00000000
 d0    ffffffff   d1    00000000   d2    0006f9b3   d3    00000077
 d4    00000003   d5    70be0077   d6    00000009   d7    ffff4caf
 a0    000fd104   a1    000ffdcb   a2    000ffaff   a3    000ffd54
 a4    00002f9e   a5    000ffb3c   a6    00002f3c   ssp   000ffaec
 sr    2500       pc    00f1e24e

 PDT >
```

```
                                                  Knob = Scroll
 ▸Cursor 1 = Addr_Strb   +3890000 ps     +5.244 V
  Cursor 2 = Addr_Strb   +3700000 ps   +260.000 mV
  Cursor ▲ =             190.000 ns       4.984 V
```

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CIRCLE NO. 131

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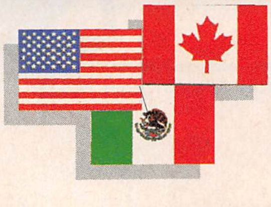
Part of the NCR SCSI Development Team: (left to right) **Jerry Armstrong**, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.



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San Jose, CA 95110
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Here's another.

The NCR 53C700 SCSI I/O Processor… So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip… for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

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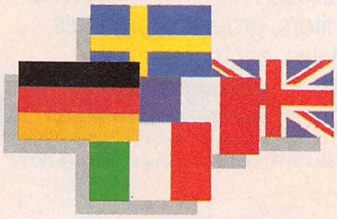
NCR

Creating value

CIRCLE NO. 110



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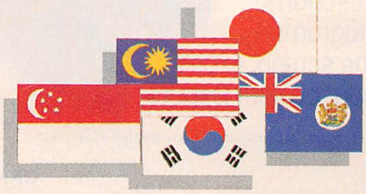

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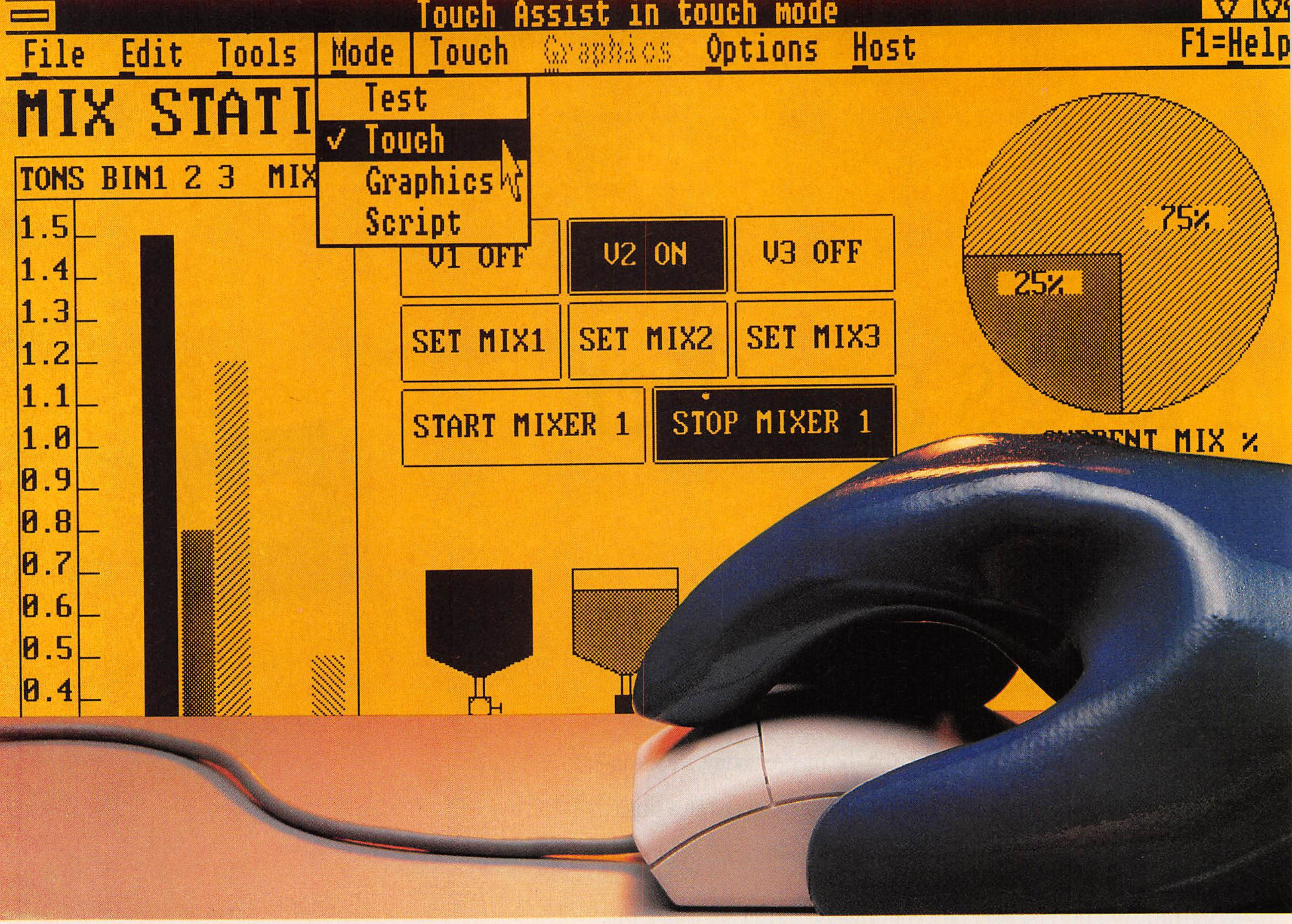

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CIRCLE NO. 151

HYPERSTONE

32-BIT CMOS

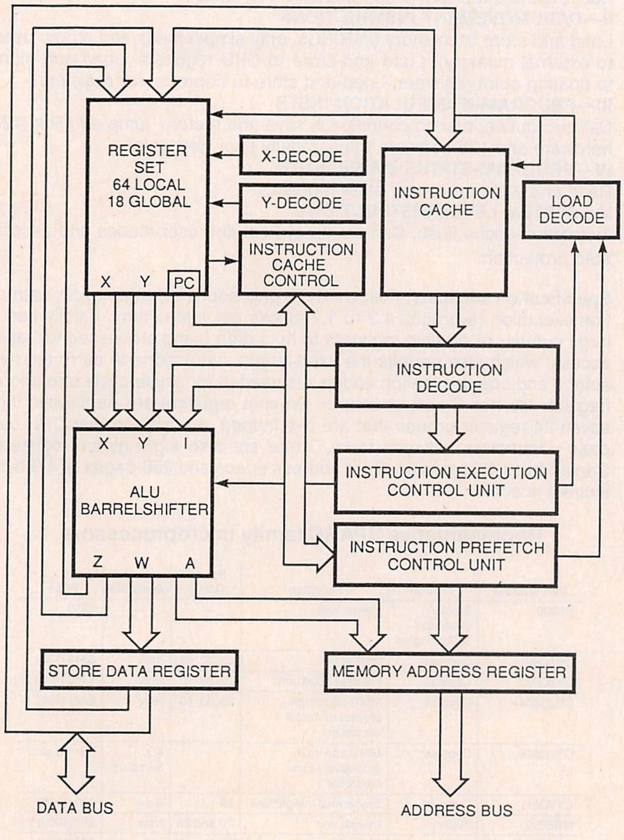
AVAILABILITY: Delivery from stock.
COST: $150 (1000) for the 25-MHz part.
SECOND SOURCE: Zilog.
CORE: Zilog will use the Hyperstone µP as a 32-bit core in its library of µP cores.

Hyperstone Electronics GmbH
AM Guckenbühl 10
7750 Konstanz
Germany
Phone (011) 49 075 316-7789
For more information, Circle No. 392

Description: Hyperstone combines features of both RISC and CISC architectures. Although most instructions are 16 bits wide, some are 32 or 48 bits wide. Almost all instructions execute in a single cycle. The vendor claims that Hyperstone program code will be more compact than many CISC-architecture programs. The microprocessor uses a combination of pipelined load instructions, an internal decode/execute pipeline of two stages, and a proprietary look-ahead instruction cache to achieve high performance. In addition, on-chip DRAM and bus control simplify the interface between the µP and memory and peripherals.

Status: The Hyperstone suits embedded-systems applications. Zilog recently announced its intention to use the Hyperstone in its library of µP cores. These cores form the base for microcontrollers for datacommunications, intelligent-peripheral-control, and disk-control applications.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The µP has separate 32-bit address and data buses. The µP's 64 local registers are arranged in a register stack that contains stack frames of variable length—2 to 16 registers. Overlapping stack frames (windows) allow parameter passing. Because of the code compaction of mostly 16-bit instructions, the 128-byte instruction cache achieves hit rates comparable to larger caches on other devices.
2. The µP contains all the logic to directly control DRAMs, SRAMs, ROMs, and other peripherals. The Hyperstone also performs parity generation and parity check.

I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on 32- or 64-bit data. Most instructions are single cycle, but multiply and divide are multicycle. A barrel shifter provides left/right and signed/unsigned shifts. Two sets of arithmetic instructions are available: One set traps on overflow; the other only flags overflow. Logic instructions are AND, AND NOT, OR, XOR, and NOT. More powerful instructions include scaled index move, bound check, and scan leading zeros. IEEE-floating-point instructions execute by emulation.
II—DATA-MOVEMENT INSTRUCTIONS
Pipelined load/store architecture. Data types are byte and halfword (both signed and unsigned), 32-bit words, and 64-bit double words. Hyperstone contains single- and double-word move instructions.
III—PROGRAM-MANIPULATION INSTR
One unconditional and 12 conditional branch instructions provide program-counter relative delayed/undelayed branches. The µP executes dynamic branches via move or add instructions to the program counter. A call instruction creates a new variable-length stack frame in the register stack. A frame instruction restructures the stack frame for parameter passing. A return instruction returns control and restores the old stack frame. The µP handles overflow or underflow automatically.
IV—PROGRAM-STATUS-MANIP INSTR
One unconditional and 11 conditional trap instructions trap to supervisor state via a 64-entry table.
V—SYSTEM-LEVEL INSTRUCTIONS
Moves to special registers and setting the interrupt mask bit are only possible in supervisor mode.

Specification summary: The Hyperstone µP has a balanced set of instructions that make it useful as a universal processor. Since virtual memory is rarely used in embedded systems, Hyperstone doesn't include on-chip memory management. Demand paging via an off-chip memory-management unit is assisted.

HARDWARE — SUPPORT — SOFTWARE

In-circuit emulator via an add-on board to the IBM PC. Add-on boards to the IBM PC and evaluation boards via an RS-232C port.

Cross assembler/debugger on the IBM PC under MS-DOS. A C compiler is under development. Zilog is developing a behavioral model.

SPARC FAMILY

32-BIT CMOS

AVAILABILITY: See table.

COST: See table.

SECOND SOURCE: Fujitsu, Cypress, and BIT SPARC µPs are not hardware compatible. LSI Logic makes Fujitsu—and Cypress—compatible versions. All must run Sun Microsystems Inc (Mountain View, CA) SPARC software. Fujitsu, Cypress, LSI, Texas Instruments, and Philips/Signetics also provide SPARC embedded controllers.

CORE: Fujitsu has made a start in this direction with a gate array. LSI Logic will also offer RISC elements in its ASIC library.

Status: L64811 supersedes the L64801. At least three vendors have signed up to produce SPARCstation 1 compatibles. Currently, more than 2000 applications run on SPARC hardware and numerous Sbus plug-in cards are available. SPARC International (Sunnyvale, CA), a consortium of hardware and software vendors, creates and maintains open standards and multivendor compatibility of both SPARC-based machines and applications.

Fujitsu Microelectronics Inc
Advanced Products Div
50 Rio Robles
San Jose, CA 95134
Phone (800) 523-0034
FAX (408) 943-9293
For more information,
Circle No. 393

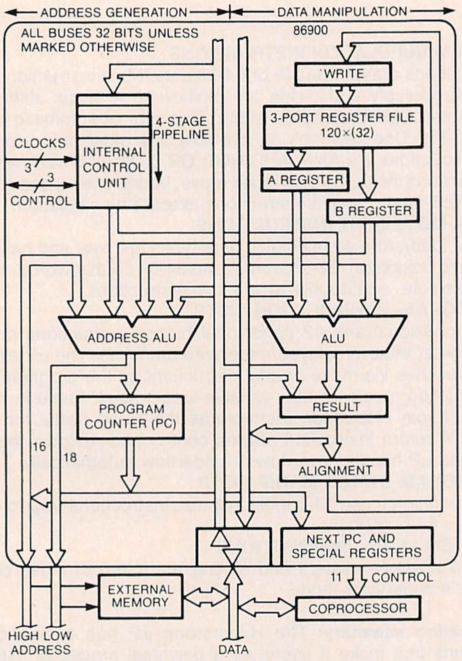
Cypress Semiconductor
3901 N First St
San Jose, CA 95134
Phone (408) 943-2852
For more information,
Circle No. 394

Bipolar Integrated Technology (BIT)
Box 4750
Beaverton, OR 97076
Phone (503) 629-5490
For more information,
Circle No. 395

LSI Logic Corp
1551 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 954-4985
For more information,
Circle No. 396

Description: Sun Microsystems defined SPARC at instruction-set and programmer's model level and then entered into entirely separate joint agreements with silicon vendors with the intent of reaching 100-MIPS performance by 1990.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:

1. Diagram is for Fujitsu 86901. 86902—Fujitsu's embedded-control entry—is compatible with 86920 MMU and Weitek's 3170 floating-point unit. 86902 is missing 3 address-space-identifier lines and 3 of 4 hold inputs.
2. Cypress's SPARC embedded controller eliminates the user-defined coprocessor port and several control signals in addition to reducing the address bus to 24 bits and the address-space identifier to 3 bits.
3. LSI Logic's embedded SPARC comes without coprocessor ports.
4. Rather than redesigned parts, all embedded controllers are reduced-pin-count, crippled versions of existing parts.

Software note:
There are four stages (five in BIT µP) of pipelining. Optimizing compiler prevents pipeline breaks by inserting a delay instruction before branch instructions.

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step). Logicals and shifts.

II—DATA-MOVEMENT INSTRUCTIONS
Load and store to memory (in RISCs, only simple loads and stores used to external memory). Load and store to CPU registers. Load and store to floating-point registers. Load and store to coprocessor registers.

III—PROGRAM-MANIPULATION INSTR
Call subroutine, branch conditional, save and restore, jump and link (128 hardware and 128 software traps, mostly user definable).

IV—PROGRAM-STATUS-MANIP INSTR
Read and write processor state register.

V—SYSTEM-LEVEL INSTRUCTIONS
Instruction-cache flush. Can set up system and user modes and associated protection.

Specification summary: Follows RISC philosophy of single-cycle instruction execution (averages 1.3 to 1.7 clocks per instruction). Family has a large number of on-chip registers to hold data being processed for rapid access, which also permits the fixed-length instructions to carry the two source and one destination addresses needed for single-cycle operations (register file has 3-port structure). On-chip registers are partitioned into seven 24-register groups that are overlapped at edges so that CPU can pass parameters between them. There are also eight global registers. Can address 4G bytes of direct address space and 256 pages of 4G-byte indirect space.

Representative SPARC family microprocessors

Part number	Vendor	Function	Speed (MHz)	Available	Price
B5000	Bipolar Integrated Technologies	Integer unit	—	—	$850
CY7C601	Cypress	Integer unit	25, 33, 40	Now	$349 (100)
CY7C602	Cypress	Floating-point unit	25, 33, 40	Now	$489 (100)
CY7C604	Cypress	MMU and single-processor cache controller	25, 33, 40	Now	$491 (100)
CY7C605	Cypress	MMU and multi-processor cache controller	—	4Q Samples	Not yet set
CY7C611	Cypress	Embedded integer unit	25	Now	$76 (1000)
MB86901	Fujitsu	Integer unit	20 and 25	Now	$87 (1000)
MB86902	Fujitsu	Embedded integer unit	20 and 25	Now	$79 (1000)
L64801	LSI Logic	Fujitsu-compatible integer unit	25	Now	$148 (1000) PQFP
L64811	LSI Logic	Cypress-compatible integer unit	25 40	Now Dec '90	$160 (1000) $223 (1000)
L64901	LSI Logic	Embedded integer unit	20 and 25	Taking orders now	$86 (1000) 20-MHz PQFP
L64951	LSI Logic	System controller	10 and 25	Samples now	$79 (1000) 20-MHz PQFP
TMS390C602A	TI	FPU	40	Samples now	$315 (1000)

HARDWARE — SUPPORT — SOFTWARE

Sun workstations are adequate because Sun maintains software compatibility. Evaluation boards from Cypress and Fujitsu. Definicon and CAD/CAM International supply development boards. Call Cypress for company phone numbers. LSI Logic has a hardware-support program supplying a SPARCstation 1-compatible board with complete schematics, layouts, and films.

Vendors say they'll pass along Sun's optimizing compilers for C, Pascal, and Fortran as well as Sun's Unix operating system. Wind River Systems (Emeryville, CA) will provide a real-time operating system. A SPARC monitor is available from Bradley Forthware (Sunnyvale, CA).

0.99 Power Factor Corrected Switcher With Universal Input

1000 watt single and multiple output switch-mode power supplies operate from 120 VAC 15 Amp service, or as Universal Input from 90 to 264 VAC line without strapping. Units meet IEC 555-2 harmonic distortion and UL, CSA, VDE, EN, and FCC safety and EMI specifications. Other models operate from 48 VDC or 120/230 VAC.
Contact: **Qualidyne** (619) 575-1100

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Compact power supplies can provide up to 400 watts with hundreds of volt/amp combinations of from 1 to 7 DC outputs. Units are available with in-line or side-mount I/O terminals and operate from 120/230 VAC. Options include Auto Current-Sharing with a isolated Power Supply Fail signal, ideal for N+1 use.
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Qualidyne CIRCLE NO. 161

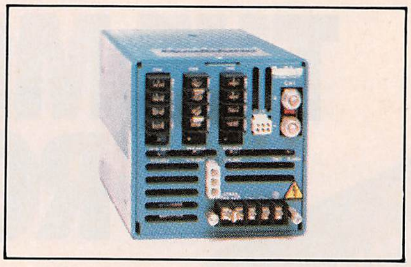
Low Profile/Low Cost Supplies Are Only 2" to 3" High

Compact switchers feature robust, high-current main and auxiliary outputs to suit OEM needs. Single and multiple output models provide from 250 to 1000 watts. Wide user-adjustment ranges, auto AC line select, integral fan-cooling, margining, and inhibit are among the features and available options.
Contact: **Qualidyne** (619) 575-1100

Qualidyne CIRCLE NO. 162

Modular 5" x 5" & 5" x 8" AC-DC Switchers & DC-DC Converters

Hundreds of models with up to 9 independent outputs can be easily configured to meet custom requirements without delays. Providing 800 to 3000 watts, units operate from 48 VDC or 120/230 VAC. All meet EMI and safety specs from UL, CSA, EN, FCC and VDE. Wide adjustable and current sharing outputs available.
Contact: **Qualidyne** (619) 575-1100



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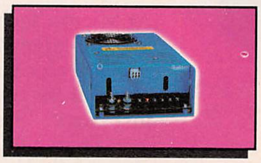
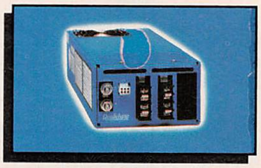


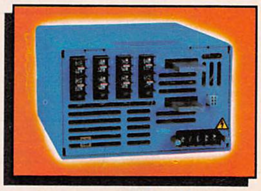
- User-Configurable
  - 1 to 9 Outputs
    - Quick Customized Supplies
      - Modular Construction

- Feature-Intensive
  - Low Profile Cases
    - 1 to 9 Outputs
      - 500 to 1000 Watts



- Wide Adjustment Ranges
  - 600 to 1000 Watts
    - 2V to 56VDC Outputs
      - 1 to 7 Outputs

- 1KW to 3KW
  - 1 to 9 Outputs
    - N + 1 Redundancy



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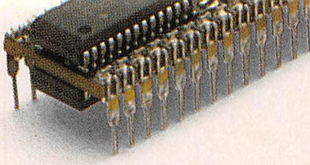

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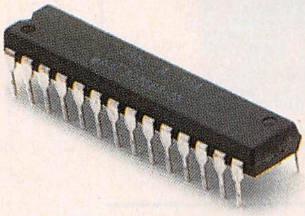

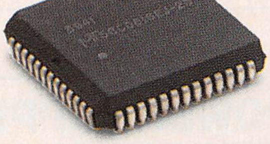

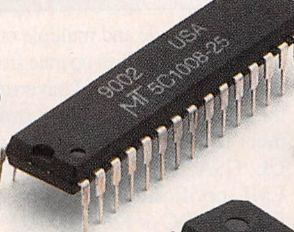

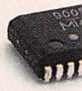

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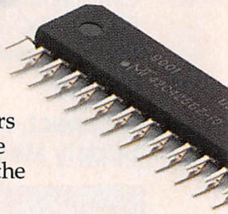

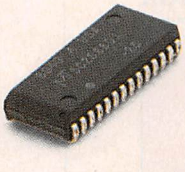

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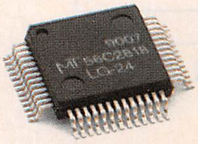
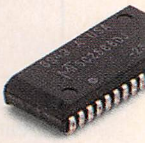
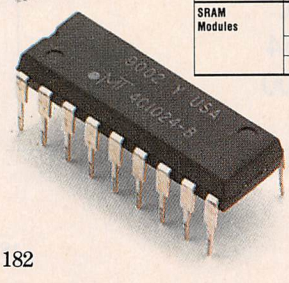
Component Product Family	Memory Size (Total)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SOJ	PLCC	TSOP	PQFP			
SRAMs	1MEG	x1,x4,x8	25-45	X		X				x4 option: OE	Now	2H90
	256K	x1,x4,x8	20-45	X	X	X				x4 option: OE	Now	X
	64K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
	16K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
Cache Data SRAMs	288K	x9	14-34				X			486 Compatible, Self-timed write, Fast toe 7ns, 486 Burst and extended burst support	Samp: 1H91, Prod: 2H91	
	144K	x18	20-35				X		X	386/486 Compatible, Fast toe 8ns, Auto write completion, Parity bits	Now	
	128K	x16	20-35				X		X	386 Compatible, Fast toe 8ns	Now	
Synchronous SRAMs	288K	x18	15-25				X			Registered address, chip enables and write control; Data latch, Fast toe 6ns, Byte write capability	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-25				X					
SRAMs with Address Latch	288K	x18	15-35				X			Address, data and chip enable latches; Byte write capability, Fast toe 6ns, 3.0 Volt output buffer option	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-35				X					
	16K	x8	100	X		X				Intel 8051 and 8096 compatible	Now	X
	16K	x8	15-35	X		X				Compatible with high end micro controllers	Now	X
FIFOs	18K	2Kx9	15-35	X			X			Family options: 300 mil DIP package, Programmable flags	Samp: 1H91	2H91
	9K	1Kx9	15-35	X			X				Samp: 1H91	2H91
	4.5K	512x9	15-35	X			X				Samp: 1H91	2H91
DRAMs	4MEG	x1,x4,x8,x16	60-100	X	X	X		X		x4,x8 options: Write per bit x16 options: 2 WE/1CAS; 1WE/2CAS and 1WE/1CAS with write per bit	x1,x4 Samp: Now, Prod: 1H91; x8,x16 Samp: 1H91	Samp: 1H91
	1MEG	x1,x4,x16	70-120	X	X	X		X		x16 options: Byte write or write per bit	Now	X
	256K	x1,x4	100-120	X	X	X	X				Now	X
	64K	x1	100-150	X			X				Now	X
Quad CAS DRAMs	4MEG	x4	60-100			X				Separate CAS control for each DQ input/output, Enhanced write per bit capabilities	Samp: 1991	
	1MEG	x4	70-100			X					Now	
Pseudo Static DRAM	1MEG	x8	80-120	X		X		X		Unmultiplexed addresses, Simple refresh control	Samp: 2H90, Prod: 1H91	
Dual Port DRAMs (VRAMs)	1MEG	x4,x8	80-120		X	X				CMOS, Fully static SAM, Serial input, Split read transfer	Now	Samp: 1H91
	256K	x4	100-120	X	X					CMOS, Fully static SAM, Serial input	Now	X
Triple Port DRAMs	1MEG	x4,x8	80-120			X	X			CMOS, Two fully static SAMs, Transfer mask, Split transfers, Functional superset of 1MEG VRAM	Samp: Now, Prod: 2H90	

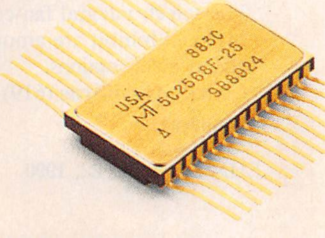
Module Product Family*	Word Size (Words)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SIP	SIMM					
DRAM Modules	2MEG,1MEG, 512K,256K	x36	70-120		X		X			Industry standard pin-out	256K, 512K: Now; 1MEG, 2MEG Samp: 2H90	
	4MEG,1MEG, 256K	x9	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	4MEG,1MEG, 256K	x8	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
SRAM Modules	256K, 128K, 64K, 16K	x32	15-45		X					Industry standard pin-out with OE	16K, 64K: Now; 128K,256K: 2H90	1H91
	64K,32K	x16	30-45	X						Industry standard pin-out with OE	Now	1H91
	128K	x8	30-45	X						Compatible with 1MEG monolithic	Now	1H91

* Custom module and board-level product manufacturing services available.









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2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3900

CIRCLE NO. 96

R2000/R3000 FAMILY

32-BIT CMOS

AVAILABILITY: See table.
COST: See table
SECOND SOURCE: NEC.

Description: This RISC architecture was initially developed at Stanford University under the auspices of DARPA (Defense Advanced Research Projects Agency). The architecture supports as many as three tightly coupled processors.

Status: The R2000, R3000, and R3000A are multisourced, specification-compatible RISC µPs. Such workstation companies as Digital Equipment Corp, Silicon Graphics, Sony, and MIPS have selected the architecture as the one to build their RISC-based hardware on. The R3000 was selected by JIAWG (Joint Internal Avionics Working Group) as a standard for military avionics programs such as the Advanced Tactical Fighter.

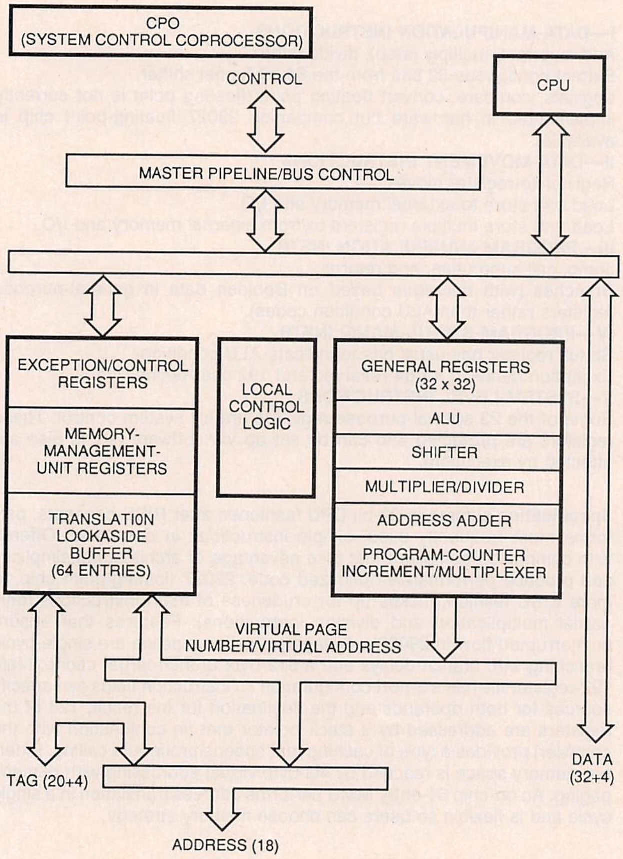
Integrated Device Technology
3001 Stender Way
Santa Clara, CA 95052
Phone (408) 492-8333
For more information,
Circle No. 397

LSI Logic Corp
1551 McCarthy Blvd
Milpitas, CA 95035
Phone (408) 433-7556
FAX (408) 433-7447
For more information,
Circle No. 398

Performance Semiconductor
610 E Weddell Dr
Sunnyvale, CA 94089
Phone (408) 734-8200
For more information,
Circle No. 399

Siemens Components Inc
2191 Laurelwood Rd
Santa Clara, CA 95054
Phone (408) 980-4500
For more information,
Circle No. 400

HARDWARE — CHARACTERISTICS — SOFTWARE


CPO
(SYSTEM CONTROL COPROCESSOR)
CONTROL
CPU
MASTER PIPELINE/BUS CONTROL
EXCEPTION/CONTROL REGISTERS
MEMORY-MANAGEMENT-UNIT REGISTERS
TRANSLATION LOOKASIDE BUFFER (64 ENTRIES)
LOCAL CONTROL LOGIC
GENERAL REGISTERS (32 x 32)
ALU
SHIFTER
MULTIPLIER/DIVIDER
ADDRESS ADDER
PROGRAM-COUNTER INCREMENT/MULTIPLEXER
VIRTUAL PAGE NUMBER/VIRTUAL ADDRESS
TAG (20+4)
DATA (32+4)
ADDRESS (18)

Hardware note:
Diagram reflects R3000 architecture.

I—DATA-MANIPULATION INSTRUCTIONS
Implements classic RISC load-store architecture where all data-manipulation operations occur on data in internal registers at the rate of one operation per cycle. Add, subtract, and logical operations, as well as multibit shifts, comparisons, and multiply and divide operations are in 3-operand format.

II—DATA-MOVEMENT INSTRUCTIONS
External memory is only accessed for simple loads and stores. Load and store to CPU registers. Processor supports loading and storing of unaligned 32-bit data.

III—PROGRAM-MANIPULATION INSTR
Processor contains a rich set of instructions for program manipulation and operating-system kernels. Has coprocessor interface to the MMU to support the virtual-memory system. The processor also contains instructions to manage program-control flow.

IV—PROGRAM-STATUS-MANIP INSTR
Exceptions can be initiated by interrupt, memory-access faults, and the floating-point coprocessor and are tracked by in-system control registers.

V—SYSTEM-LEVEL INSTRUCTIONS
Bits in the status register let the processor modify the system interface in order to perform memory-system diagnostics.

Specification summary: The R2000/R3000 implements a 5-stage pipeline to achieve a low average-clocks-per-instruction rate. Rich instruction set, sophisticated compilers, and high-frequency operation help the R2000/R3000 family achieve high performance. The IDT 79R3000 features a full cache controller, including on-chip tag comparison and direct control of the cache RAMs. LSI Logic's LR2000/3000/3000A includes thirty-two 32-bit general-purpose registers, on-chip cache control, on-chip memory management, and coprocessor interfaces for as many as three external coprocessors.

Representative R2000/R3000 family microprocessors

Part number	Vendor	Speed (MHz)	Price
79R3000	Integrated Device Technology (IDT)	12.5–33	As low as $50
LR3001	IDT	12.5–33	As low as $50
LR2000	LSI Logic	12.5–16	$99 (100)
LR3000*	LSI Logic	16–25	$144 (100)
LR3000A	LSI Logic	To 33	$400 (100)
R2000	Siemens	12.5–16	$252 (100)
R2010	Siemens	12.6–16	$347 (100)
R3000	Siemens	20–25	$335 (100)
R3010A	Siemens	20–25	$447 (100)
R3051	IDT	20–40	$30 (10,000) General sampling in early 1991
R3052	IDT	20–40	$49 (10,000) General sampling in early 1991

*MIL versions available

HARDWARE — SUPPORT — SOFTWARE

MIPS Computer Systems offers several machines for system development. The architecture is supported by a variety of tools, including logic-analysis tools from Tektronix, Arium, and Gould. IDT offers a line of CPU subsystems. IDT and LSI Logic also offer a range of development systems.

LSI Logic and IDT provide C, Ada, Pascal, Fortran, Cobol, and PL/1 compilers for their CPUs. LSI also offers the System Programmers Package, an integrated toolkit for software and hardware development.

The operating system RISC/OS is a merged AT&T System V.3 and Berkeley BSD 4.3 Unix including TCP/IP and NFS networking software. It includes the MIPS optimizing compiler as well as the MIPS symbolic debugger.

Refer to the RISCware directory from Synthesis Software Solutions Inc for a complete list of third-party software vendors.

29000 FAMILY

32-BIT CMOS

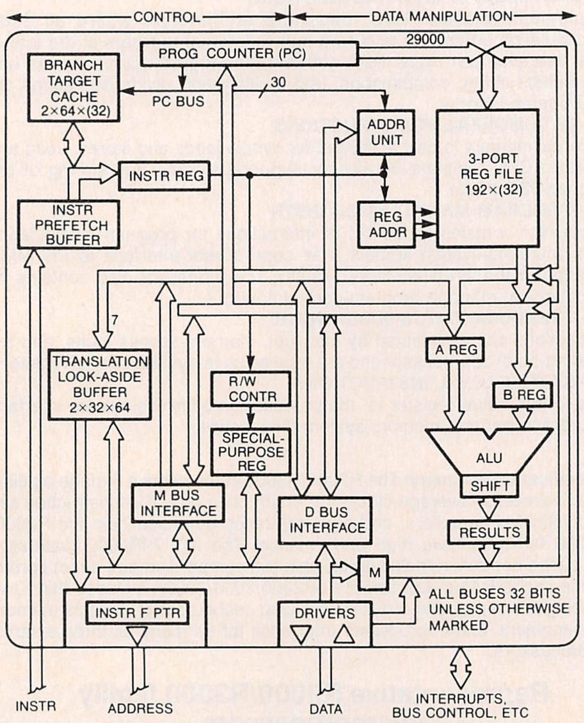
AVAILABILITY: Now for 29000 CPU and 29027 arithmetic accelerator.
COST: $88 for the 16-MHz 29000, $68 for the 16-MHz 29005, and $268 for the 16-MHz 29027 (1000). Parts are also available in 20- and 25-MHz grades.
SECOND SOURCE: Under negotiation.

Description: State-of-the-art implementation of RISC µP concepts with expected stress on obtaining as close to single-cycle operation as possible (even with branching) and an emphasis on keeping users' system costs down by bus timing, etc, which allows lower-cost external memories. Although their names are similar, the 2900 and 29300 building-block families are intended for user-defined (microcoded) complex instruction sets, whereas the 29000 µP family has a regular, fixed, and purposely simple instruction set; moreover, the instruction set is decoded by logic. Companion compilers are an essential part of family.

Advanced Micro Devices (AMD)
901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400
For more information, Circle No. 401

Status: In the 2½ years since its introduction, the 29k has accumulated over 200 design wins, and 35 companies have announced 29k-based products. Areas of particular success for the RISC µP are high-end laser printers; X-terminals; graphics, including graphics controller boards, graphics accelerators, real-time image processing, and medical imaging; and network products, including protocol converters, network node controllers, FDDI networks, and ISDN-related systems.

HARDWARE — CHARACTERISTICS — SOFTWARE



I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step), divide (step).
Extract contiguous 32 bits from the 64-bit funnel shifter.
Logicals, compare, convert floating point (floating point is not currently implemented in hardware but companion 29027 floating-point chip is available).
II—DATA-MOVEMENT INSTRUCTIONS
Register-to-register moves.
Load and store to external memory and I/O.
Load and store multiple registers to/from external memory and I/O.
III—PROGRAM-MANIPULATION INSTR
Jump, call subroutine, and returns.
Branches (with decisions based on Boolean data in general-purpose registers rather than ALU condition codes).
IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition.
Exception handling for 64 reserved and 192 user-defined traps.
V—SYSTEM-LEVEL INSTRUCTIONS
Some of the 23 special-purpose registers are for system control. These registers are protected and can be set up via software (some also are affected by execution).

Specification summary: 32-bit CPU fashioned after RISC concepts; performs most frequently used, simple instructions in one cycle. Offered with companion compilers that take advantage of architectural simplicity and produce performance-optimized code. 29027 floating-point chip, in more CISC fashion, makes up for crudeness of math instructions (only partial multiplication and division instructions). Features that ensure uninterrupted flow in 29000's 4-stage execution pipeline are single-cycle branching with branch delays and a 512-byte branch-target cache. Main 192-register file has a 3-port configuration so instruction fields can specify sources for both operands and the destination for the result. 128 of the registers are addressed by a stack pointer that (in conjunction with the compiler) provides a type of caching that speeds procedure calling. External memory space is reached by 4G-byte virtual addressing with demand paging. An on-chip 64-entry MMU performs address translation in a single cycle and is flexible so users can choose memory strategy.

Hardware notes:
1. Burst-mode addressing allows use of lower-cost video RAMs to replace more-expensive, high-speed, static CMOS RAMs, with only moderate loss in performance (14 MIPS sustained vs 17 MIPS).
2. There is a coprocessor interface to companion 29027 floating-point chip. The 29027 uses combinatorial logic, so operations take only five 29000 cycles.

Software notes:
1. Total of 115 instructions. All are not yet implemented in hardware; those that aren't cause traps.
2. Multiply and divide on the 29000 only does one step. The full multiply and divide instruction causes a trap operation at which a compiler can insert a software routine.

HARDWARE — SUPPORT — SOFTWARE

The EB29k is a PC plug-in execution board with software-development tools.
From others: Embedded Performance Inc, Hewlett-Packard, and Step Engineering all provide real-time in-circuit emulators for the 29000 family. Logic Analyzer interface is available from Biomation or Hewlett-Packard. Various VMEbus board products based on the 29k are available from Ironics. Behavioral simulation models are available from Logic Automation and Mentor Graphics. Design-verification and test-generation models are available from Teradyne. A list of third-party support products appears in the biannual Fusion29K Catalog published by AMD.

AMD supplies the complete software tool chain. These tools include the ANSI standard HighC29k optimizing compiler with an assembler, linker, and ANSI standard libraries; floating-point-math libraries; and architectural and instruction-set simulators. The Xray29k source-level debugger is also available for the 29k. The Mon29k is a target debug monitor for system developers. All software support tools run on IBM PC/ATs and Sun-3 and Sun-4 workstations.
Other C compilers are available from Embedded Performance Inc, Metaware, Microtec, and Intermetrics. Pascal compilers are available from Metaware. The GNU tool chain, including the G++ and the debugger are available from Cygnus. Ada is available from Verdix Systems. Fortran is available from Yarc. Ready Systems, JMI, and Telenetworks provide real-time operating systems. A complete guide to third-party software products is published in the biannual AMD Fusion29k catalogue.

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CIRCLE NO. 106

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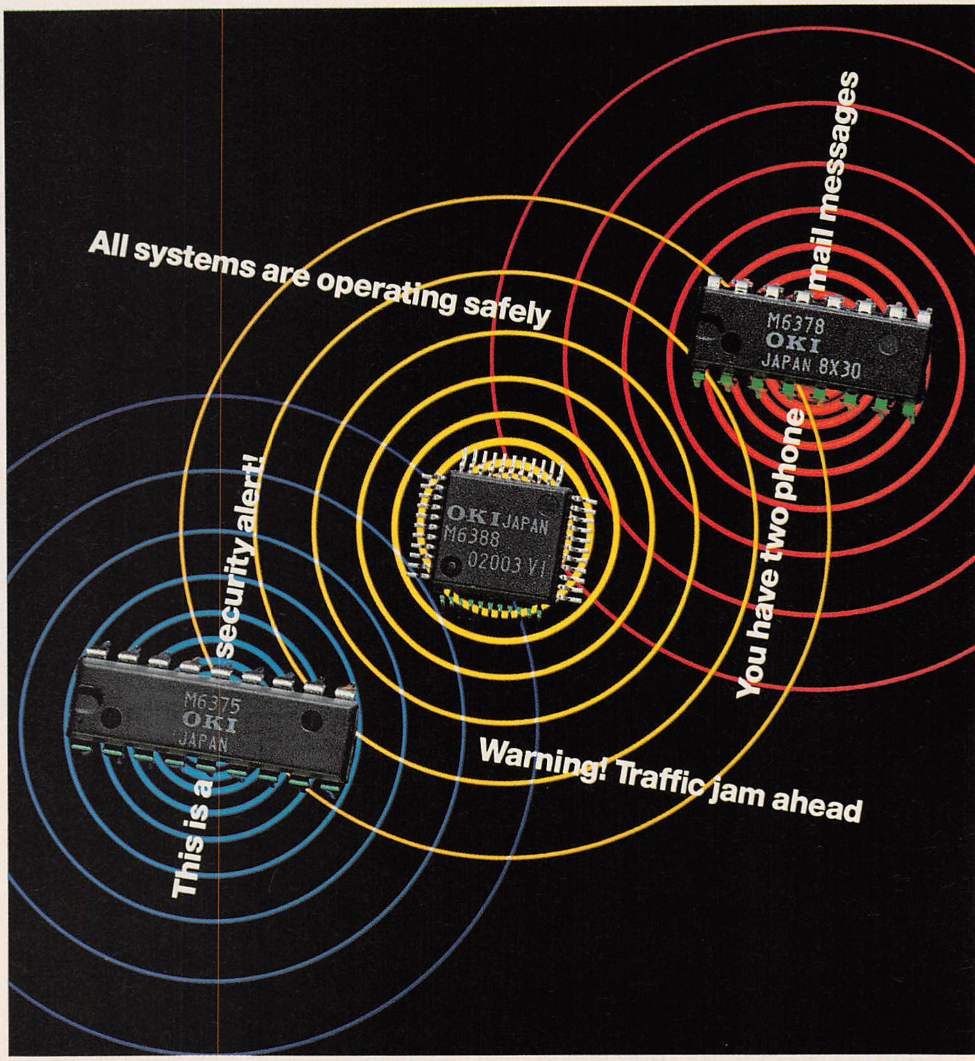
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CIRCLE NO. 105

88000 — 32-BIT CMOS

AVAILABILITY: Both the 88100 CPU and the 88200 cache/memory-management unit (CMMU) are available now in 16-, 20-, 25-, and 33-MHz versions.

COST: The 88100 costs $168; the 88200 costs $198 (100).

SECOND SOURCE: None.

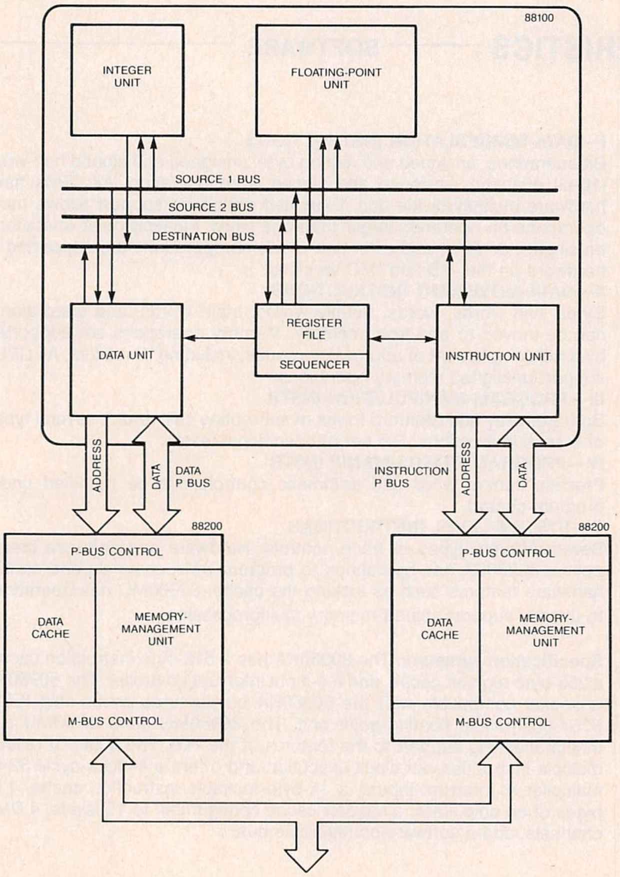
CORE: Motorola's architecture can incorporate as many as six special-function units into the 88100 chip.

Description: The 88000 RISC family encompasses the 88100—the CPU—and the 88200—the memory-management unit. The 88100 chip supplies full 32-bit registers, data paths, and addresses. Most instructions, including standard IEEE-P754 floating-point math operations, execute in one cycle or are put in a concurrent execution pipeline in one cycle. The corresponding 88200 cache/memory-management unit supports a demand-paged virtual-memory environment. The chip controls two 4G-byte logical address spaces—one for the user and one for the supervisor. The chip's architecture supports multiprocessor operations.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 928-6000
For more information, Circle No. 402

Status: The 88000 µP family is designed into such applications as PC add-in cards, disk controls, imaging systems, and real-time controllers. An independent group of manufacturers has founded the 88open Consortium Ltd (San Jose, CA) to support and promote the µP family. The consortium develops standards such as the Binary Compatibility Specification, which allows applications written for the 88000 to execute on all 88000 hardware.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. Architecture shown is for the 88100. The CMMUs are shown in block-diagram form.
2. The P bus supplies the interface between the 88100 and either local memory or an 88200 CMMU. The synchronous P bus operates at the same clock rate as the 88100. Peak data rate is 80M bytes/sec.
3. The 88100 includes 32 general-purpose registers.

I—DATA-MANIPULATION INSTRUCTIONS
Integer-math instructions include add, subtract, divide, multiply, and compare. There are equivalent floating-point instructions as well as integer-float conversion, store, exchange, round, and truncate instructions. The instructions also provide logical and bit-field operations.

II—DATA-MOVEMENT INSTRUCTIONS
The basic data-movement instructions let the CPU load registers, addresses, and the control register's contents. The CPU can also store information and exchange the contents of registers and memory. The instruction set includes operations that move data within the floating-point unit.

III—PROGRAM-MANIPULATION INSTR
These instructions include conditional and unconditional branch, jump, and subroutine-call commands. The 88100 also provides trap instructions that check bit locations, memory boundaries, and interrupt conditions.

IV—PROGRAM-STATUS-MANIP INSTR
The 88100 can process exceptions—those conditions that cause the processor to stop its operation and locate a potential problem. Exceptions include interrupts, memory-access faults, math errors such as divide by zero, and trap instructions.

Specification summary: The 88100 provides register-to-register operations for all data-manipulation instructions. Separate source and destination registers are available. The CPU supports register-to-register and register-plus-immediate-value address modes. Because address calculations are quick, memory-access operations are speedy, in keeping with the RISC philosophy. The CPU employs delayed branching, which reduces pipeline delays caused by a change in program flow. The 88200 incorporates 16k bytes of cache memory as well as cache-control logic, memory-management logic, and bus-control circuits. Multiple CMMUs can operate in parallel. Both the 88100 and 88200 come packaged in 180-pin PGA packages. The chips operate over the 0 to 70°C temperature range.

HARDWARE — SUPPORT — SOFTWARE

From Motorola: The company has announced a variety of VMEbus-based boards and systems.

From others: Add-in boards are available for the IBM PC/AT from Opus (Cupertino, CA), for the IBM PS/2 from Prometa (Gainesville, FL), for the Apple Macintosh from Tektronics (Beaverton, OR), for the VMEbus from Force (Campbell, CA) and Tadpole (Cambridge, UK), and for the VAX from Avalon (Santa Barbara, CA)

From Motorola: 88000 systems run Motorola's BCS/OCS Unix System V, Release 3 as well as System V, Release 4, both of which are supported by optimizing C and Fortran compilers and associated development tools for complete software development.

From others: A variety of compilers and applications are available for the 88000. See the 88open software catalog.

80960

32-BIT CMOS

AVAILABILITY: Now for 10-, 16-, 20-, and 25-MHz 80960KA and KB in PGAs; 16- and 20-MHz plastic quad flatpack (PQFP); 16-, 20-, and 25-MHz 80960MC in PGAs and QFPs; 16-, 25-, and 33-MHz 80960CA in PGA; and 16- and 25-MHz 80960CA in PQFP.

COST: Prices depend upon speed, package, and temperature range. In 1000s, prices range from $27 to $56 for the 80960KA, $35 to $73 for the 80960KB, $920 to $1058 for the 80960MC, and $81 to $122 for the 80960CA.

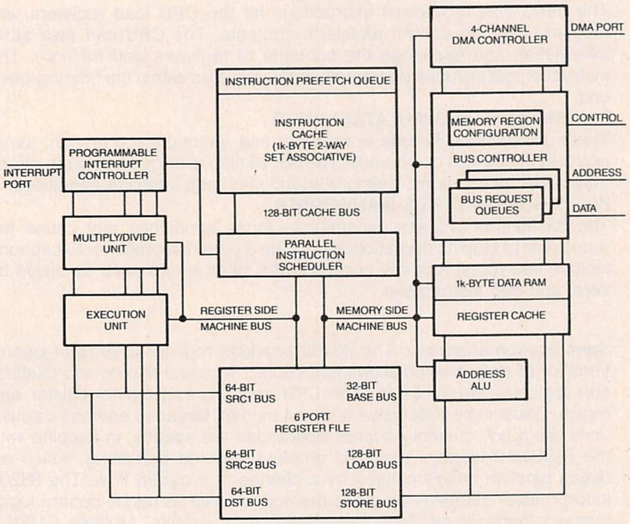
SECOND SOURCE: Internally sourced from three different Intel facilities.

Description: The 80960 is Intel's 32-bit family of μP chips that has been designed specifically for embedded-control applications. There are four upwardly compatible versions of the RISC-based architecture. The family includes the basic 80960KA core version, which provides 6 to 12 VAX MIPS (depending on frequency); the 80960KB, which includes an on-chip floating-point unit; the 80960MC, which comes with on-chip memory-management/protection and multiprocessor support; and the 80960CA, which features a software-configurable pipelined bus, 1.5k bytes of on-chip data RAM, a 1k-byte, 2-way set-associative instruction cache and a 4-channel chaining DMA processor.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 403

Status: Since the 80960 family's introduction, the family has enjoyed widespread acceptance in a broad spectrum of commercial and military designs. The 80960 family played a role in legitimizing the 32-bit embedded-control market. Intel's approach is family oriented; not only is there a wide range of 32-bit CPU chips at different price/performance levels, but there are also 80960-specific support components such as the 27960 burst EPROM and 85C960 bus control component. Intel claims the total kit approach exists to serve embedded-control customers with an easy-to-design-with set of CPU and peripheral parts.

HARDWARE — CHARACTERISTICS — SOFTWARE



Hardware notes:
1. The 80960 provides only one data bus for instructions and data. The bus multiplexes address and data information.
2. The basic 80960 chip includes 16 32-bit global registers and 16 32-bit local registers. The stack requires one global and three local registers for housekeeping operations.
3. The floating-point unit (80960KB) also includes four 80-bit registers, but can use any register.

I—DATA-MANIPULATION INSTRUCTIONS
Bit operations, unsigned and signed byte, unsigned and signed half-word (16-bit quantity), unsigned and signed word operation. All CPUs have hardware multiply/divide unit. Extended arithmetic support allows math operations on operands larger than one word. Floating-point operations on single-, double-, and extended-precision operations are supported in hardware on the -KB and -MC versions.

II—DATA-MOVEMENT INSTRUCTIONS
Bytes, half words, words, double words, triple words, and quad words can be moved to and from memory. Memory operations are supported by a full complement of addressing modes, including IP relative. All CPUs support unaligned memory operations.

III—PROGRAM-MANIPULATION INSTR
Both Berkeley and Stanford forms of subroutine call, return; several types of branch instructions. Full set of conditional tests.

IV—PROGRAM-STATUS-MANIP INSTR
Process control word and arithmetic controls can be modified under program control.

V—SYSTEM-LEVEL INSTRUCTIONS
Seven different types of trace controls. Hardware and software breakpoints. 80960CA has operations to program DMA channels and control hardware features such as locking the cache. 80960MC has operations to directly support shared-memory multiprocessing.

Specification summary: The 80960KA has a 512-byte instruction cache, a 256-byte register cache, and a 4-input interrupt controller. The 80960KB is socket compatible with the 80960KA but features an on-chip IEEE-P754-compatible floating-point unit. The 80960MC adds an MMU and multiprocessing support to the features of the -KB. The 80960CA allows multiple-instruction-per-clock execution and offers a 4-clock-cycle 32-bit multiplier, 8 interrupt inputs, a 1k-byte lockable instruction cache, 1.5k bytes of on-chip RAM, a register cache configurable to 15 levels, 4 DMA channels, and a software-configurable bus.

HARDWARE — SUPPORT — SOFTWARE

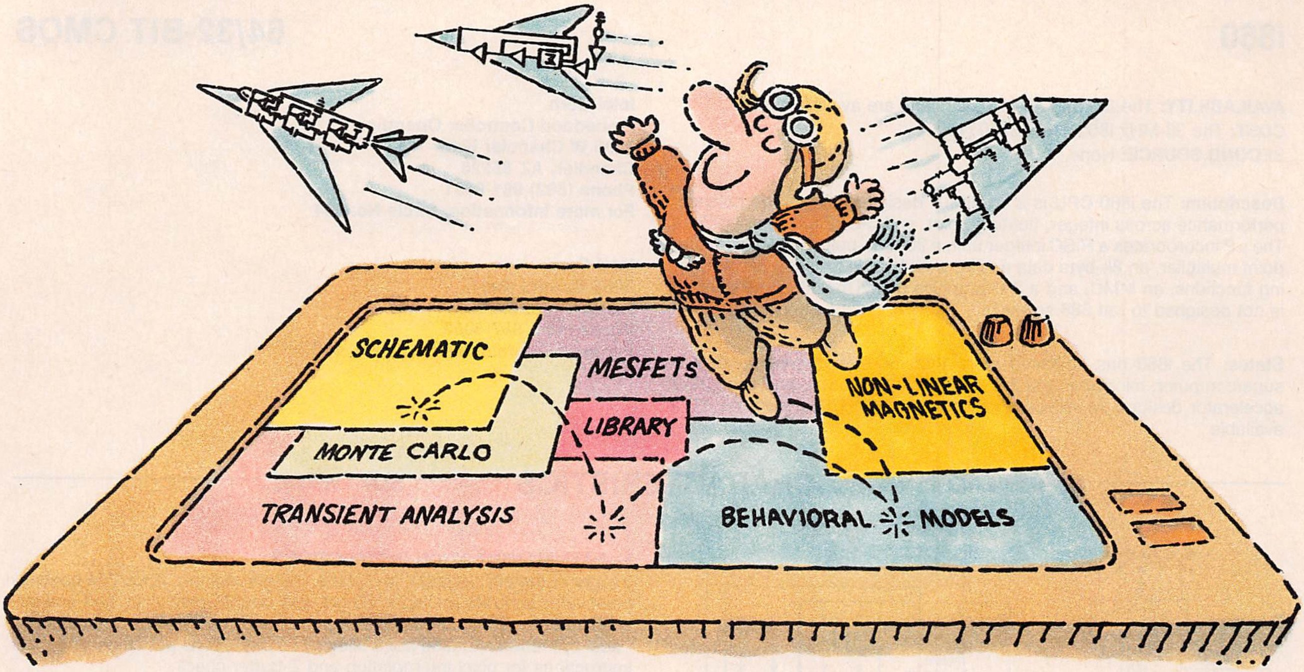
From Intel: The EVQT960E ($960) with 256k bytes of 2-wait-state memory and the EVQT960F ($1960) with 256k bytes of zero-wait-state memory are serially hosted evaluation and prototyping boards for the 80960KA/KB. The EVA960KB board ($4500) is an IBM PC/AT-compatible board with onboard debug monitor and as much as 4M bytes of dynamic RAM. The EXV960MC board ($9000) is a 25-MHz Multibus I development board for military and Ada applications. The EV960CA ($3500) is an evaluation board for the 80960CA. The ICE960KB in-circuit emulator ($16,495) is available for the 80960KA/KB.

The 85C960 is a bus-control chip for the KA/KB; the 27960CX/KX are high-speed burst EPROMs for the 80960KA/KB/CA; the 27C202 is a high-speed, 16-bit-wide EPROM for the 80960KA/KB/CA. The 82380 is a multifunction peripheral with timer-counters, 8 channels of DMA, and 15 interrupt inputs that can interface to the 80960KA/KB/MC. The M82965 is a bus-interface component that provides multiprocessing and fault-tolerance support for the 80960MC.

From others: 80960CA Multibus II boards are available from Micro Industries. 80960CA VME boards are available from Heurikon ($3995) and Tadpole. Fluke provides logic-analyzer support.

From Intel: ASM960 ($900 for the IBM PC/AT) includes an assembler and linker for the 80960 family. iC960 ($700 for the IBM PC/AT) is a full ANSI C compiler for the 80960 family. Gen960 builds memory images for the 80960KA/KB/MC/CA. Hosts include the IBM PC/AT, Sun-3, VAX/VMS VAX/Ultrix and HP9000. Ada960 (from $28,000) is available for VAX/VMS. RMK960 ($1500) is a real-time kernel for 80960KA/KB. SIM960CA ($750, IBM PC/AT) is a software simulator for the 80960CA. DB960 ($2500) is a C source-level debugger hosted on a IBM PC/AT for the 80960KA/KB/CA.

From others: Wind River Vxworks provides a full-featured operating environment that includes file-system support and TCP/IP networking. Ready Systems VRTX32 provides a deterministic real-time kernel for the 80960 family. Microtec Research provides a complete 80960 tool chain—C compiler through XRay debugger. QTC provides an instruction scheduler/optimizer for the 80960CA. The Solutions960 catalog from Intel describes additional 80960 tools and applications.



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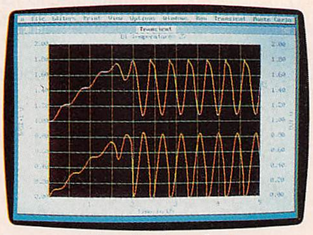
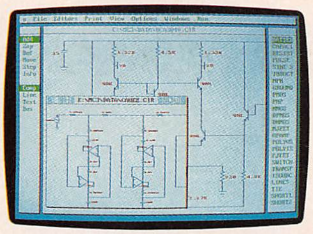
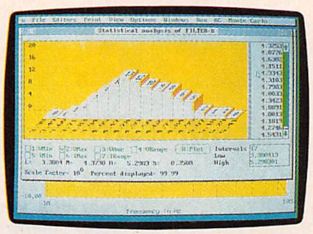


Transient analysis



Schematic editor



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CIRCLE NO. 121

i860

64/32-BIT CMOS

AVAILABILITY: The 33- and 40-MHz versions are available now.
COST: The 33-MHz i860 costs $750 (1000).
SECOND SOURCE: None.

Description: The i860 CPU is a 64-bit µP designed to provide balanced performance across integer, floating-point, and 3-D graphics operations. The µP incorporates a RISC integer unit, a floating-point adder, a floating-point multiplier, an 8k-byte data cache, a 4k-byte instruction cache, paging functions, an MMU, and a 3-D graphics unit. The i860 runs Unix but is not designed to run 386 software.

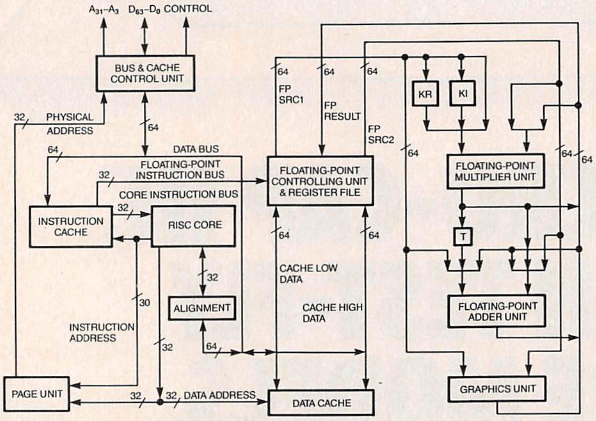
Status: The i860 has amassed more than 50 design wins to date in supercomputer, minicomputer, 3-D graphics workstation, and application accelerator designs. Multiprocessor version of Unix/System V rel 4.0 is available.

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 404

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 405

CHARACTERISTICS

HARDWARE



SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Integer arithmetic, logicals, and shifts. Integer multiply. IEEE-754 floating-point add, subtract, multiply. Single and double precision, and conversions between. Reciprocal and square-root seed instructions. Special "dual operation" floating point allows two operations per clock. Graphics instructions for pixel interpolation and Z-buffer check.

II—DATA-MOVEMENT INSTRUCTIONS
16-, 8-, and 4-byte floating-point loads and stores, with variable strides and autoincrement. 4-, 2-, and 1-byte integer loads and stores. Transfers between integer and floating-point registers. Special load instruction assists data caches. Pixel-store operation of 8 bytes.

III—PROGRAM-MANIPULATION INSTR
Unconditional and conditional branches, both delayed and nondelayed forms. Single-cycle loop-control operation. Indirect call and indirect branch. Dual-instruction mode allows execution of two instructions per clock.

IV—PROGRAM-STATUS-MANIP INSTR
Data-breakpoint register for breakpoint debugging. Big-endian mode bit switches between access modes. Cache-control bits for cache locking and testing.

V—SYSTEM-LEVEL INSTRUCTION
Lock/unlock instructions for semaphores. Flush instruction for write-back data cache. Single-cycle translation look-aside buffer and instruction cache invalidate.

Specification summary: Information not provided by manufacturer.

SUPPORT

HARDWARE

From Intel: Information not provided by manufacturer.

SOFTWARE

From Intel: Fortran and C compilers.
From Others: Industrial Programming (Jericho, NY) offers a real-time kernel, Metaware (Santa Cruz, CA) offers three varieties of High C. Green Hills (Glendale, CA) sells Fortran and C compilers, DDC-I sells an Ada compiler, and Micro Focus (Palo Alto, CA) sells a Cobol compiler for the i860.

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CIRCLE NO. 19

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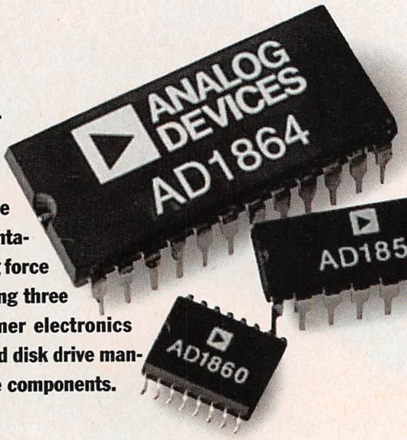

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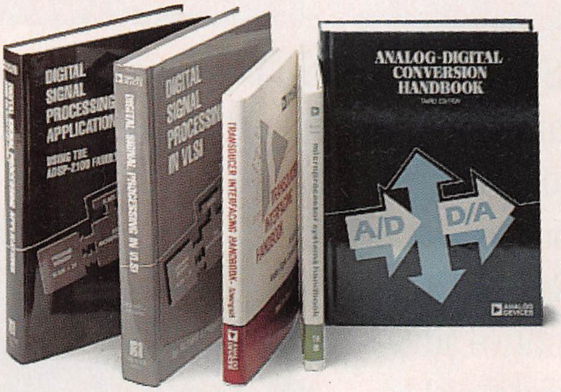
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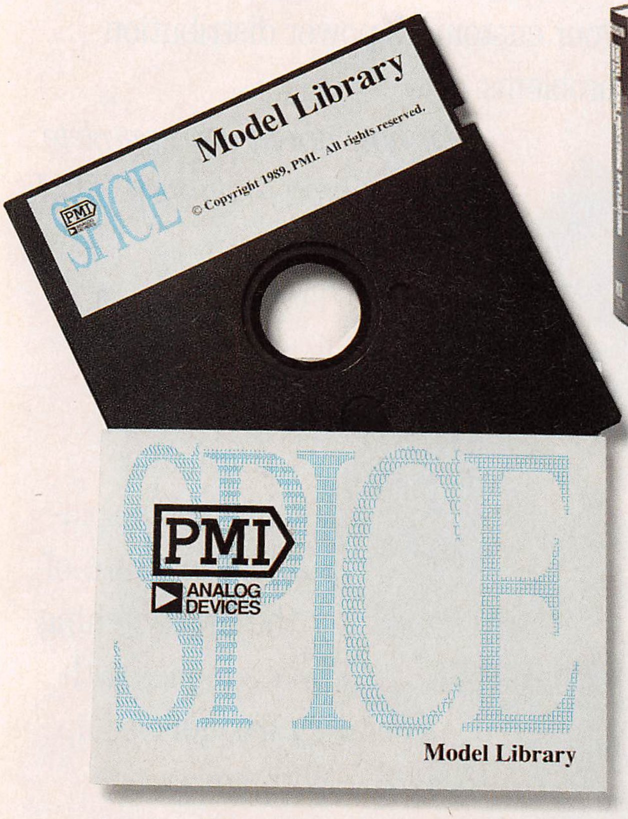

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CIRCLE NO. 144

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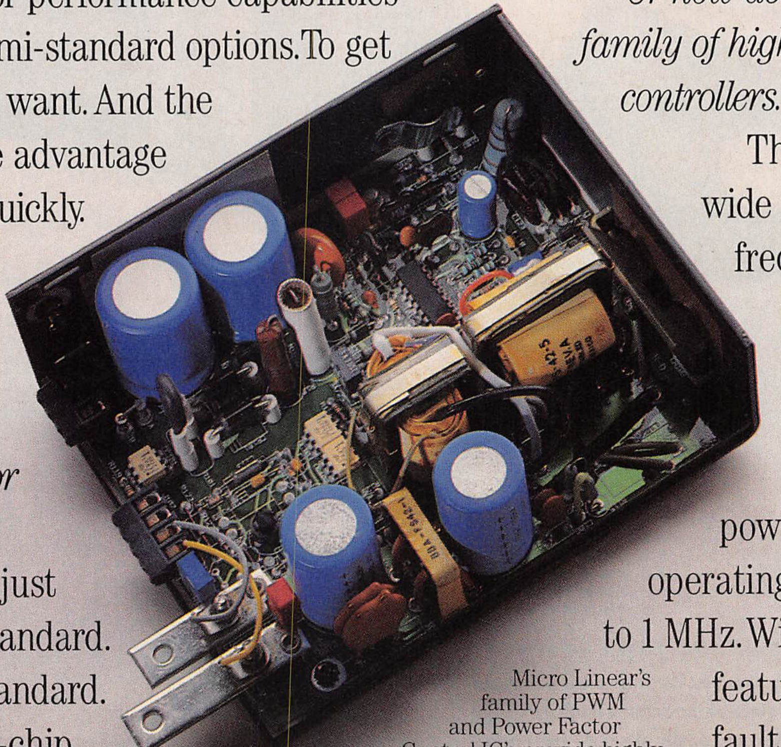

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Or how about our complete family of high-frequency PWM controllers.

They offer you a wide range of high-frequency, high-performance single chip solutions for state-of-the-art switching power supplies with operating frequencies up to 1 MHz. With advanced features like improved fault protection. Added synchronization

Product Category	Features
Power Factor Control	High Efficiency Flyback or Boost
PWM Controllers	1 MHz, Additional Fault Protection, Synchronization
Resonant Control	ZVS and ZCS to 3 MHz
Motor Control	BLDC Sensorless Commutation

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Power supply courtesy of Lamda Electronics, Inc.

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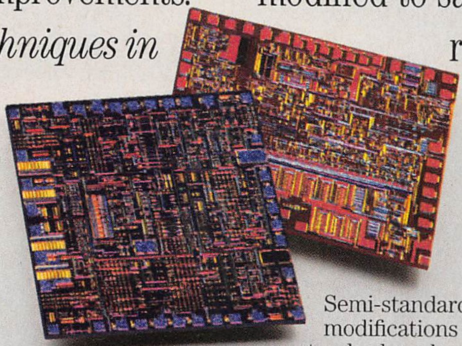

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CIRCLE NO. 111

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